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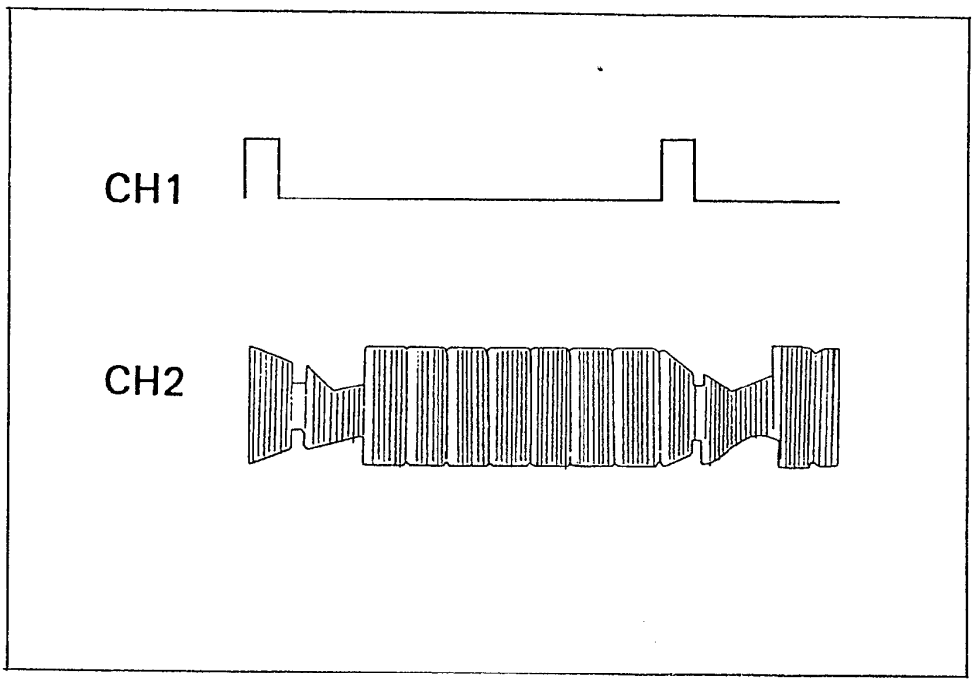
Technical Guide

Vol. 31

Auto DCC Technology



DIGITAL
dcc
COMPACT CASSETTE

Panasonic®

AUTO PRODUCTS DIVISION
Matsushita Communication Industrial Co., Ltb

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PRINCEPLES OF THE DIGITAL COMPACT CASSETTE

1. Introduction

DCC – Digital Inheritor of Compact Cassette's Role in Audio Life

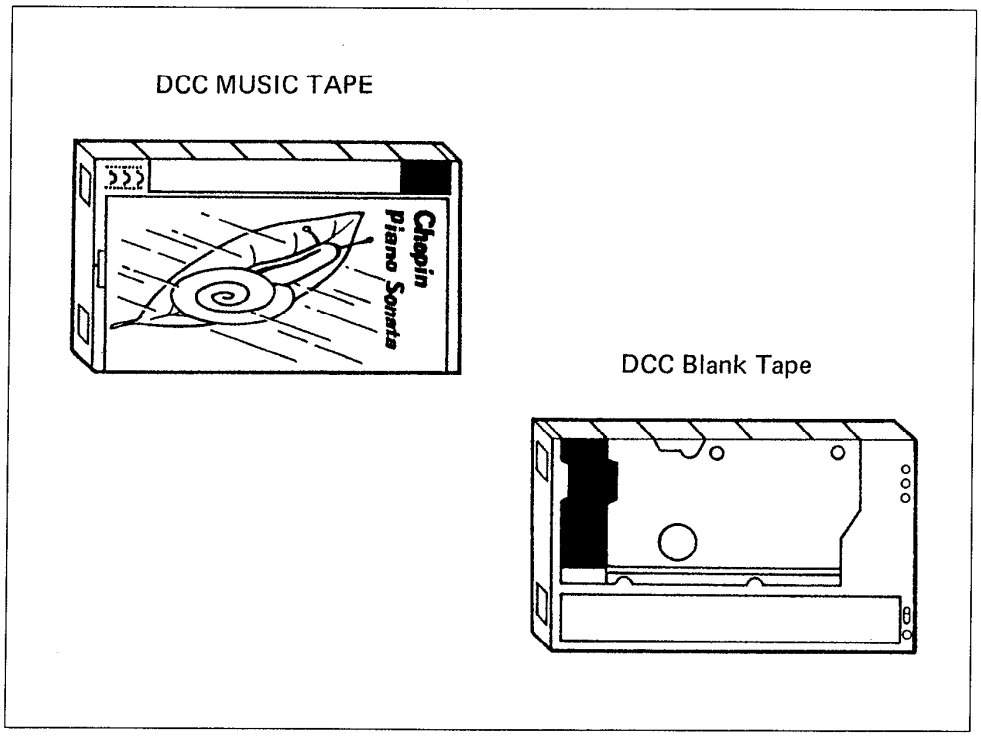
Music lovers learned to live with the scratches and noise of vinyl LPs for several decades. But when compact discs came along, the advantages were obvious. It was as if a veil had been removed, revealing a crispness and clarity that was previously enjoyable only at a live concert. And what about the cassette, that most popular of all audio media? After two decades of evolution that gradually reduced noise, raised headroom, and extended frequency response, audiophiles can now look forward to a true revolution. It's called the Digital Compact Cassette or DCC and it was announced by Philips N.V., of the Netherlands, at the 1991 Winter CES on January 9, 1991.

Behind this achievement are more than two years of collaborative development between Philips and Matsushita. As co-developers, we at Matsushita announced officially on July 5, 1991 that the development of basic technologies for DCC was completed, and that we were ready to provide any party interested with the license.

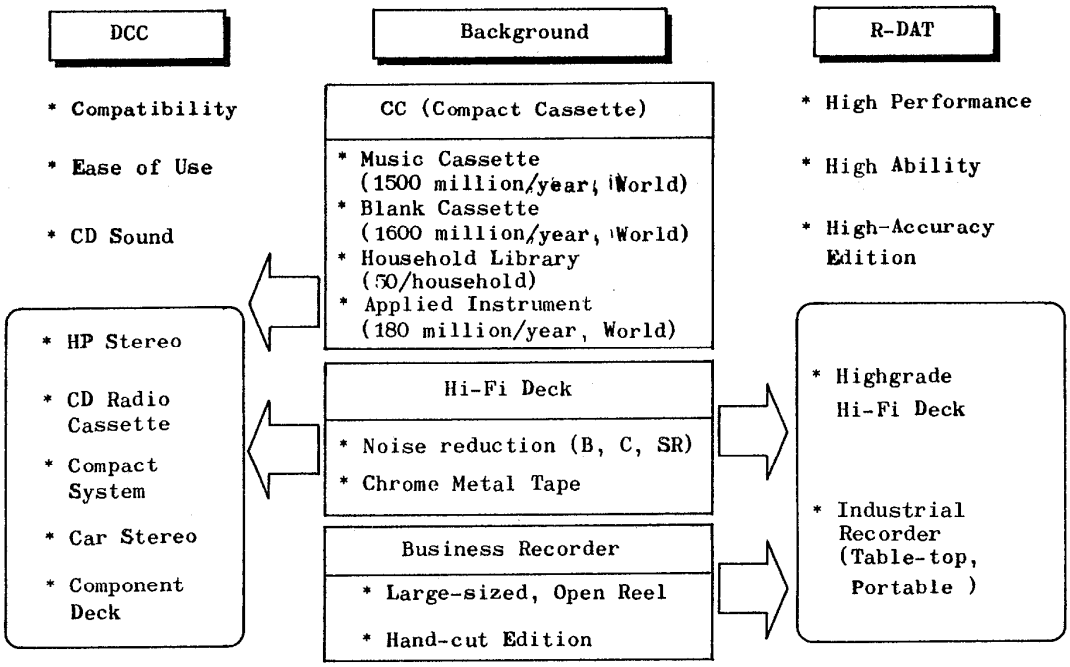
DCC is expected to inherit the role of the analog compact cassette in home audio, car audio, and personal audio applications. DCC has many of the familiar features of its predecessor, including size that matches the compact cassette. While DCC features digital sound quality and a modern high-tech look, it retains the casual convenience features that have contributed to the compact cassette's overwhelming popularity.

In fact, thanks to new technology, DCC maintains backward compatibility with analog cassettes, yet provides the sound clarity and convenient access that people have come to take for granted in today's digital formats such as the compact disc. All of this makes the DCC the most important development in audio since the compact disc was introduced eight years ago.

Support from all parts of the audio and entertainment industry is essential to the launch of a new medium. So the overwhelming cooperation of major record companies and the music industry in general augur well for DCC's success. DCC will be launched as a system. Hardware and prerecorded/blank cassettes will be available in parallel. In other words, as soon as the first DCC players and recorders are introduced, you will also have a wide and attractive array of DCC music cassette titles and blank tapes from which to choose. For these reasons we expect market penetration to surpass even that of the CD, both in terms of product quantity and rapidity of acceptance. Thanks to this new digital format's high quality sound, ease of use, and backward compatibility, the DCC revolution may prove to be one of the smoothest in audio history.



2. Background of DCC Development



3. Main Features

(1) Compatibility with Analog Cassette
- DCC player plays analog cassette, too.
- DCC mechanism has been remodeled of currently used cassette mechanism.
- Existing production equipment, improved, manufactures DCC music cassettes.

(2) Up-to-date Digital Technique
- PASC coding makes sound nearly equivalent to CD.
- Highly accurate selection of tunes by address information.
- Multi-channel stationary thin-film head.

(3) High-technology Sense & High Additional Value
- CD-like fresh cassette design.
- Lettering information including titles, song words, etc.

4. Schematic Diagram of Entire DCC

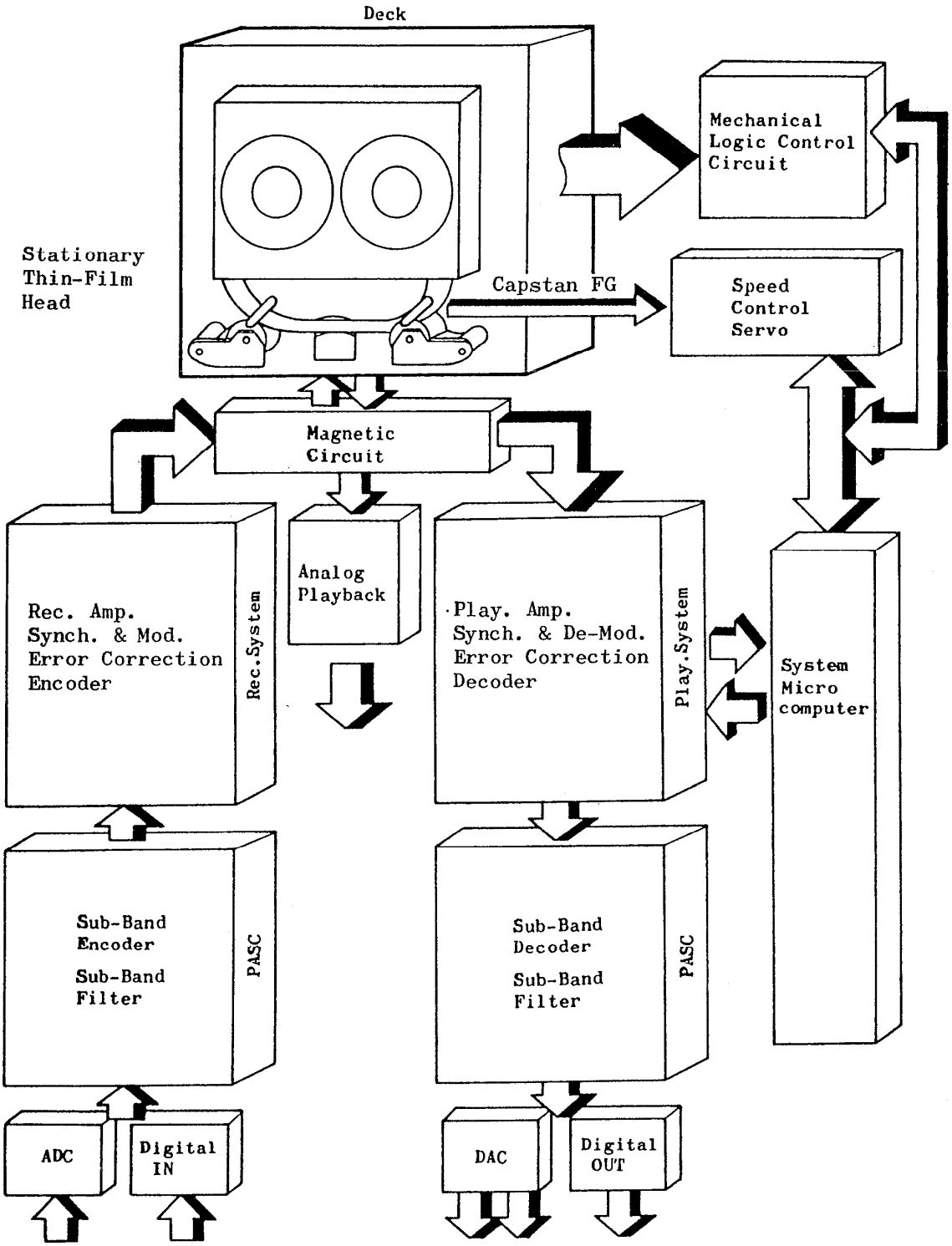


Fig. 1

5. Block Diagram and Signal Flow

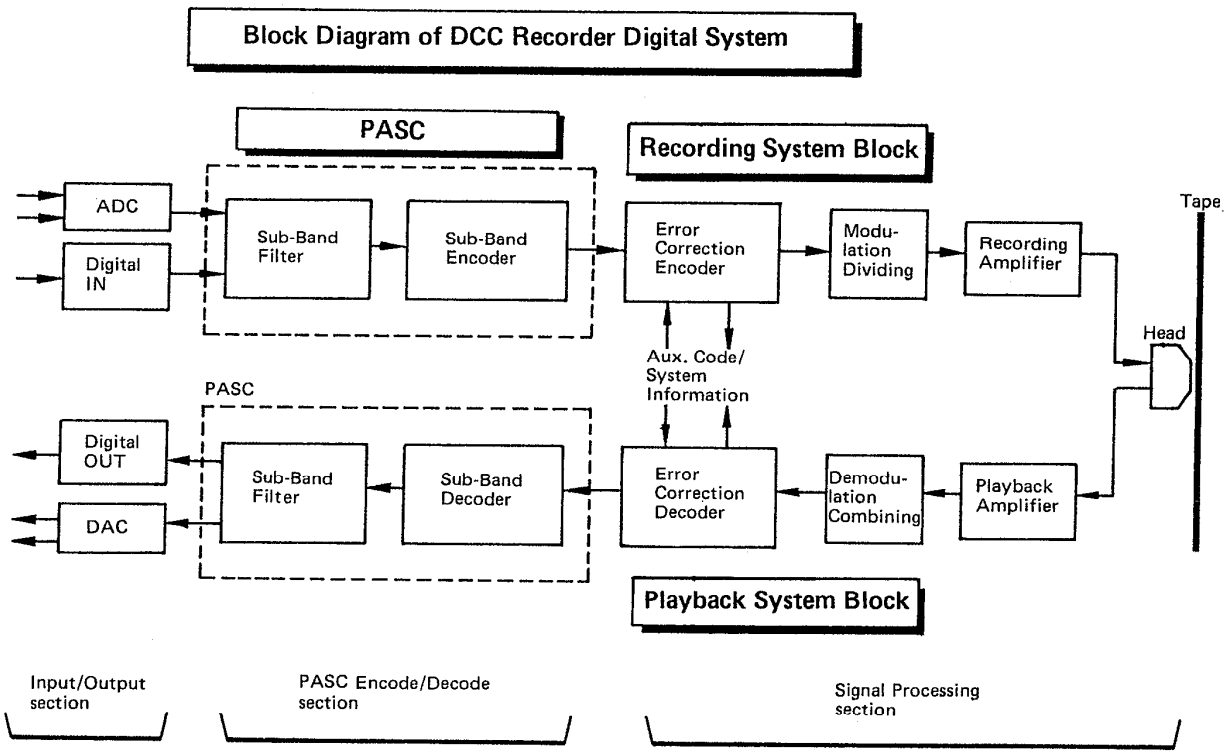


Fig. 2

Compressing data and recording on channel B:

Fig. 2 is a block diagram showing the circuit of the DCC recorder, which can be roughly divided into three components, namely Audio Signal Input/Output Section, PASC Encode/Decode Section, and Signal Processing Section.

Input/Output Part consists of A-D converter, D-A converter, and digital/audio interface circuit. Encode/Decode Part uses sub-band filters for coding, and highly efficient encoder and decoder.

Signal Processing Part comprises those circuits that are used for error detection and correction, for synchronization and synchronism detection, and for modulation and demodulation.

There are three kinds of digital signals recorded on tape and played back. They are audio signal, auxiliary code (data to control heading, etc.), and system information.

Recording and playback signals are generally processed as follows:

For recording, analog or digital input signals are divided into sub-bands, and encoded in the PASC method. To the encoded signals, error detecting/correcting signals are added. These data are divided into eight and recorded on 8 tracks simultaneously. Modulation is 8-10 conversion.

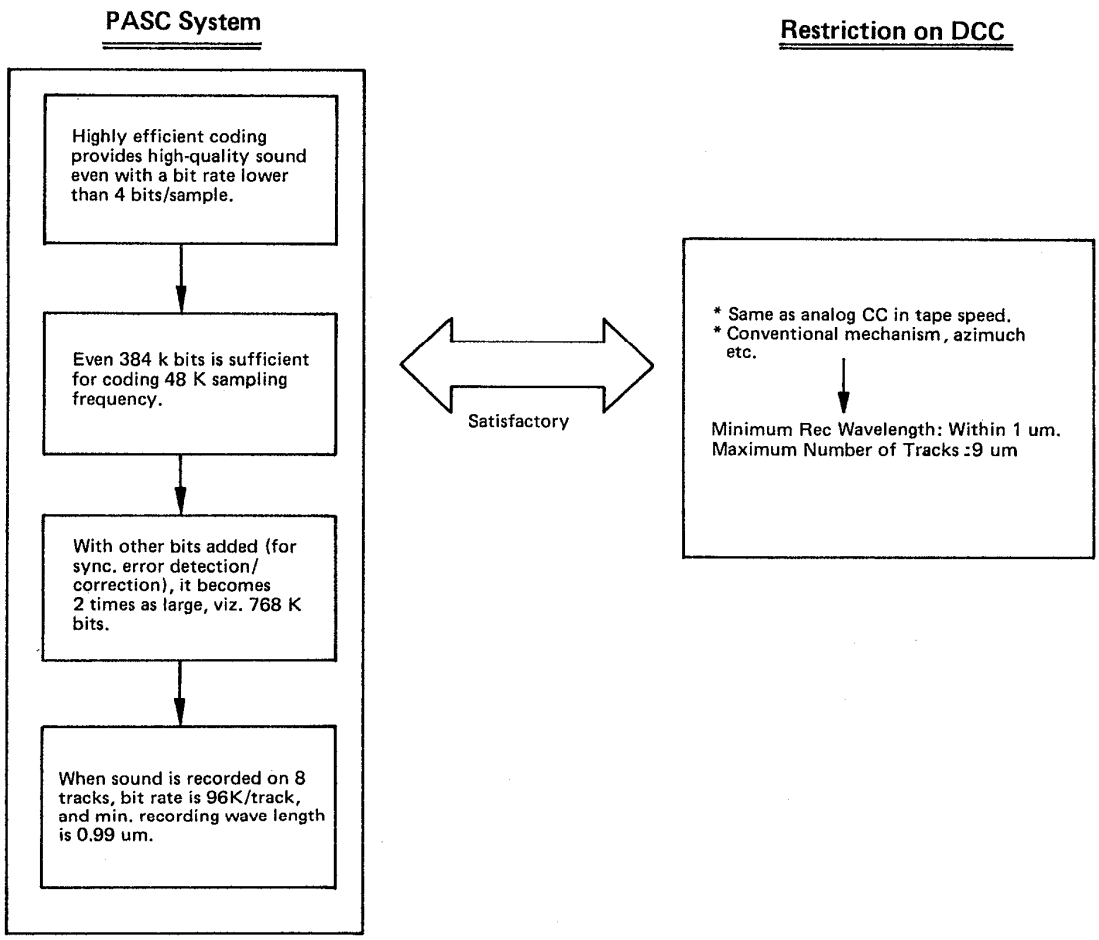
For playback, signals from tape are amplified, equalized, and then demodulated (10-8 conversion). Thereafter, errors, if any, are detected and corrected. The signals are demodulated in the PASC method. The data is output in the form of digital or analog signals.

6. PASC System

1. PASC (Precision Adaptive Sub-band Coding) Principles

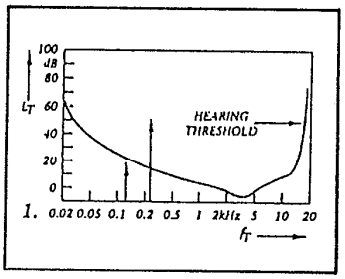
Definition ..... PASC means a kind of technique to reduce recording signals in bit rate through highly efficient coding of audio signals on the basis of the natural characteristics of the human ear.

Why is PASC requisite? ..... Because the bit rate of recording signal is restricted when it is necessary to provide interchangeability with the existing system as a feature of the DCC.


PASC System
Restriction on DCC
Highly efficient coding provides high-quality sound even with a bit rate lower than 4 bits/sample.
Even 384 k bits is sufficient for coding 48 K sampling frequency.
With other bits added (for sync. error detection/ correction), it becomes 2 times as large, viz. 768 K bits.
When sound is recorded on 8 tracks, bit rate is 96K/track, and min. recording wave length is 0.99 um.
Satisfactory
* Same as analog CC in tape speed.
* Conventional mechanism, azimuch etc.
Minimum Rec Wavelength: Within 1 um.
Maximum Number of Tracks :9 um

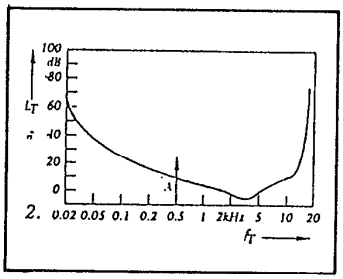
Principles of Compression

1. Man is hearing sound higher than a certain level. ---- { OK if you record at a level higher than the detection limit only.
2. Bigger sound masks smaller ones. ---- { You need not record evenly.
3. Music signals do not range to entire bands. ---- { Data is concentrated to necessary part.



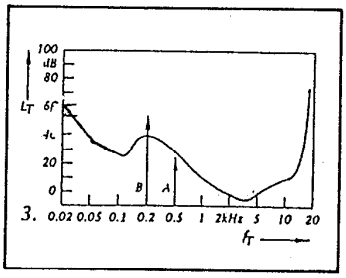
1.The threshold of hearing. Only sounds above the threshold are heard.

Fig. 3



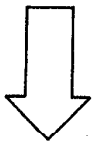
2.Soft sound (A) is audible.

Fig. 4



3.Loud sound (B) increases the threshold to an extent that masks soft sound (A). Since (A) no longer needs to be coded, extra information capacity becomes available for more precise coding of (B).

Fig. 5



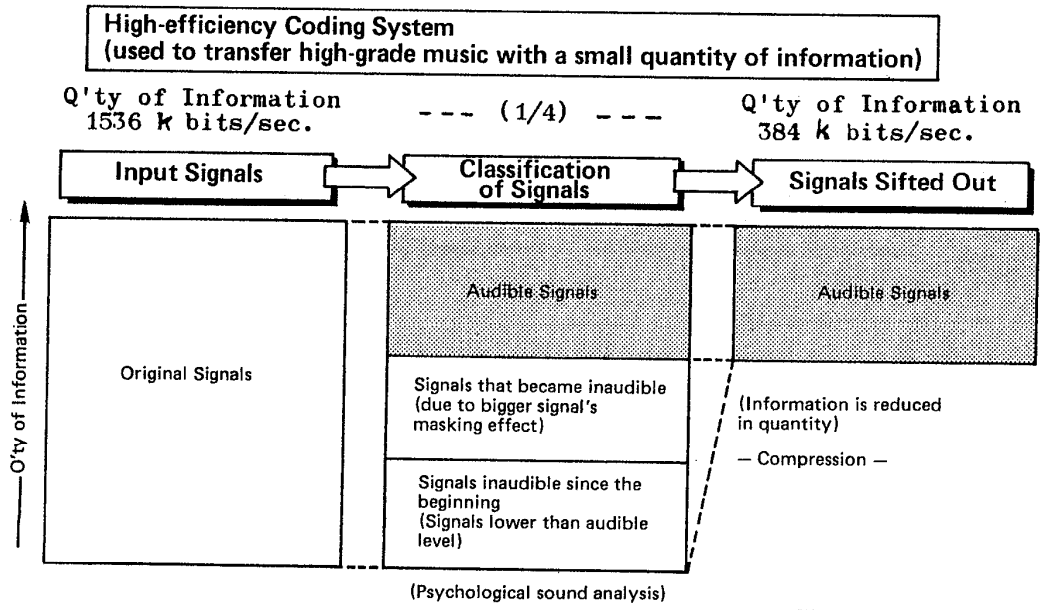
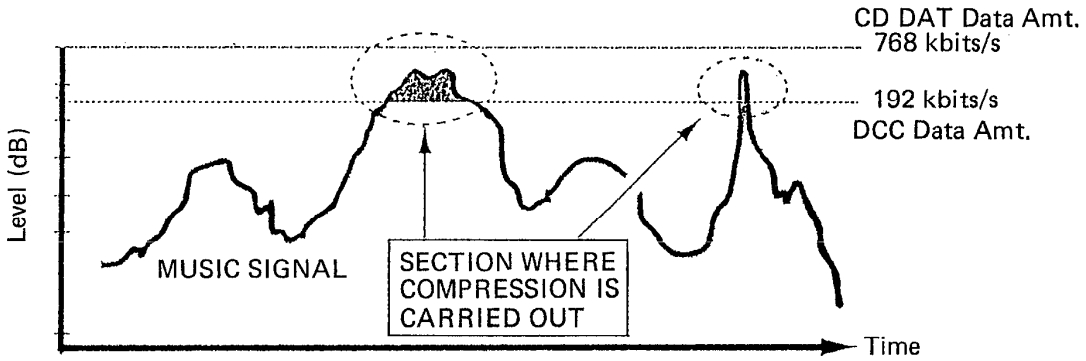

High-efficiency Coding System
(used to transfer high-grade music with a small quantity of information)
Q'ty of Information
1536 k bits/sec.
--- (1/4) ---
Q'ty of Information
384 k bits/sec.
Input Signals
Classification of Signals
Signals Sifted Out
Q'ty of Information
Original Signals
Audible Signals
Audible Signals
Signals that became inaudible (due to bigger signal's masking effect)
Signals inaudible since the beginning (Signals lower than audible level)
(Information is reduced in quantity)
– Compression –
(Psychological sound analysis)

Fig. 6

(1) CONCEPT OF COMPRESSION-1

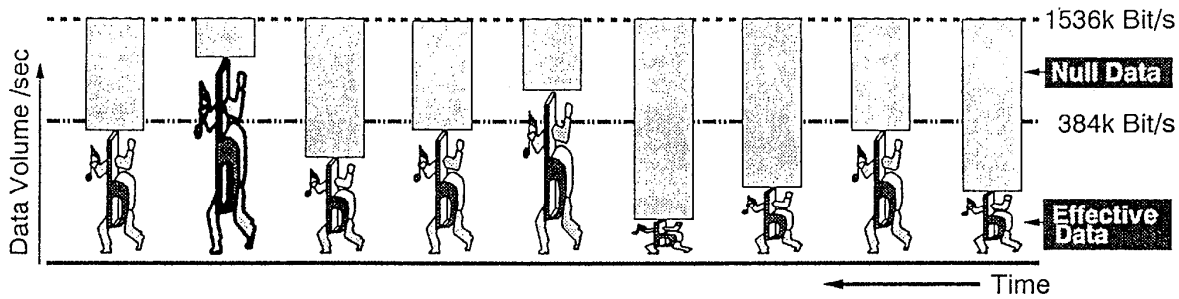
In regard to actual music signals, the amount of digital data is ordinarily such as to enable recording on a tape without the process of compression, but data compression is necessary for only those sections where the amount of digital data is too much as shown below.

RELATIONSHIP BETWEEN SIGNAL LEVEL AND COMPRESSION

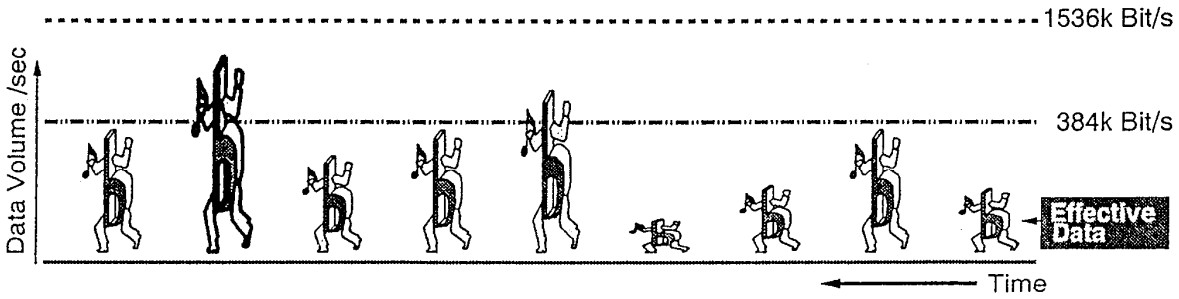


COMPRESSION TAKES PLACE WHERE SPECIFIED LEVEL OF INFO IS EXCEEDED

CD / DAT transmit both effective and null data

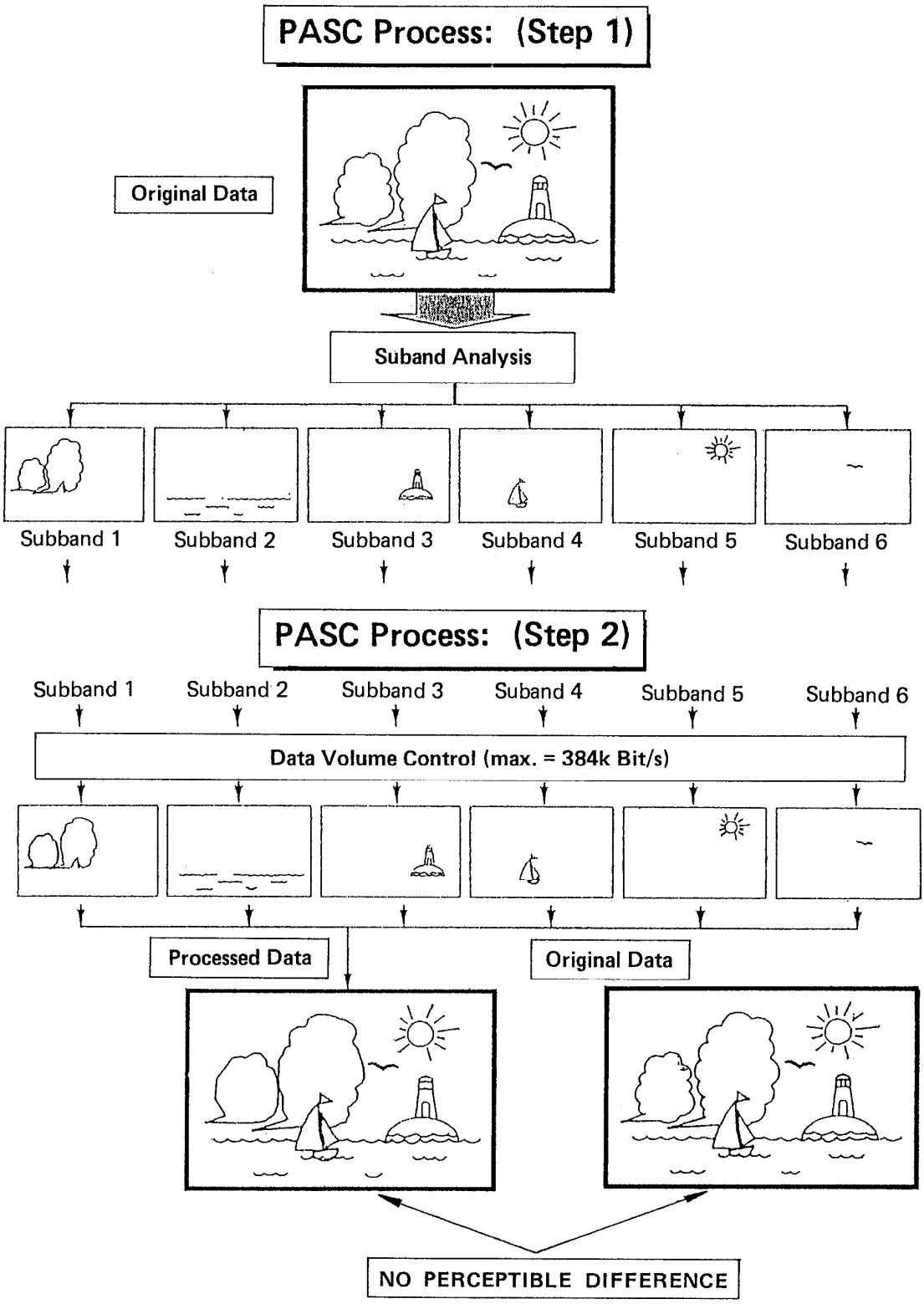


PASC transmits effective data only



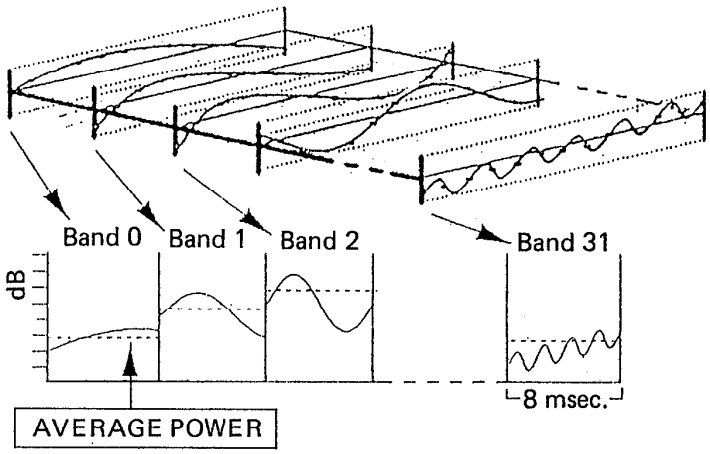
In each section where data has to be compressed, music signals centering round hardly-audible part are thinned to such an extent that almost no difference from original signal can be perceived by man's auditory sense. (Compression Process)

Given below is an example showing that the picture taken by a camera (via. after compression) does not differ perceptibly from the actual scene (original sound.)



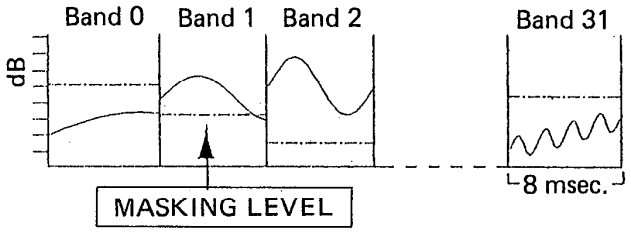
(2) CONCEPT OF COMPRESSION-2

Step 1
FREQUENCY ANALYSIS OF MUSIC SIGNALS

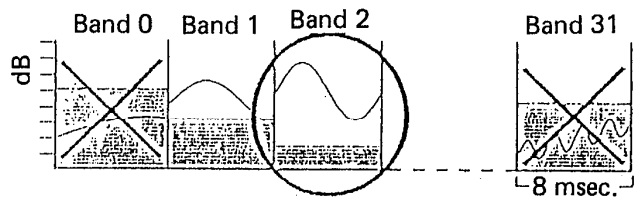


Step 2
CALCULATION OF MASKING LEVEL OF EACH BAND

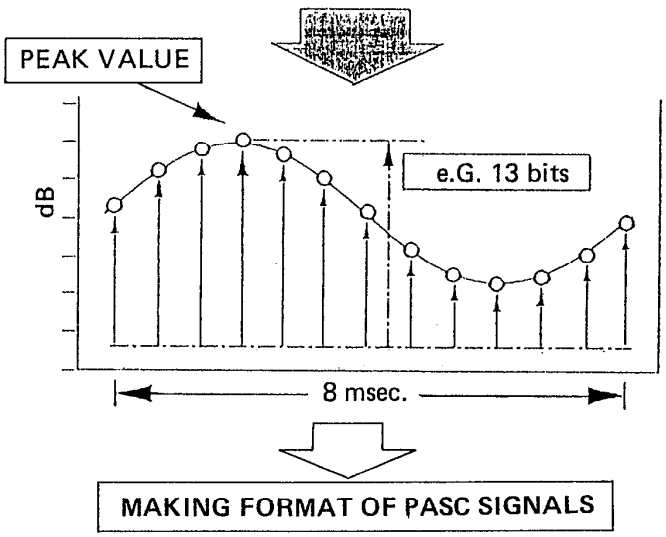
Step 3
CALCULATION OF MASKING LEVEL OF EACH BAND



Step 4
REMOVAL OF BANDS BELOW MASKING LEVEL



Step 5
CALCULATION OF QUANTIZED BITS FROM DIFFERENCE OF MASKING LEVEL



How does the PASC operate?

1. Frequency is divided into 32 bands through the digital filter.
2. Signal processor codes audible sounds only on the basis of auditory detection limit.
3. Capacity bits are apportioned to sub-bands, and unnecessary bits of any band are sub-divided to other bands as required.

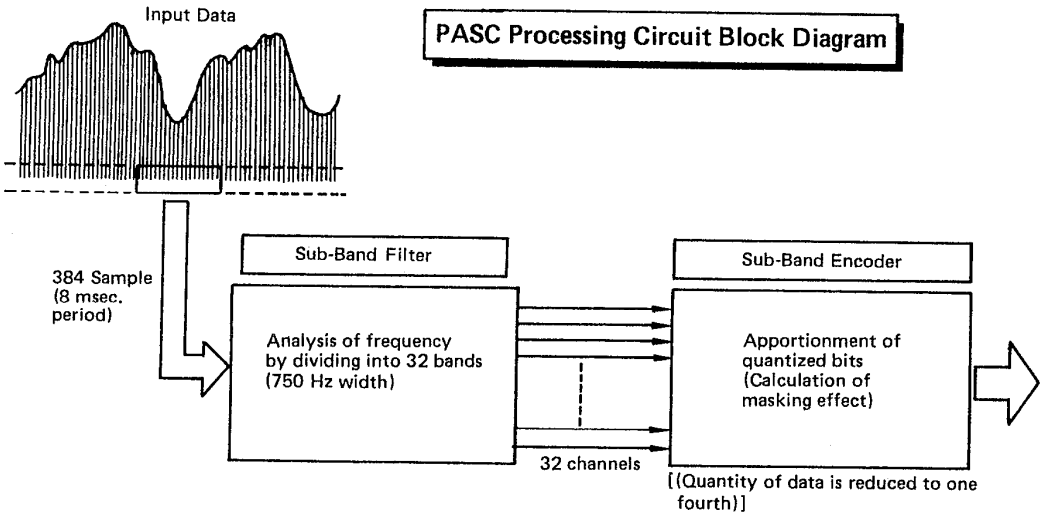


Fig. 7

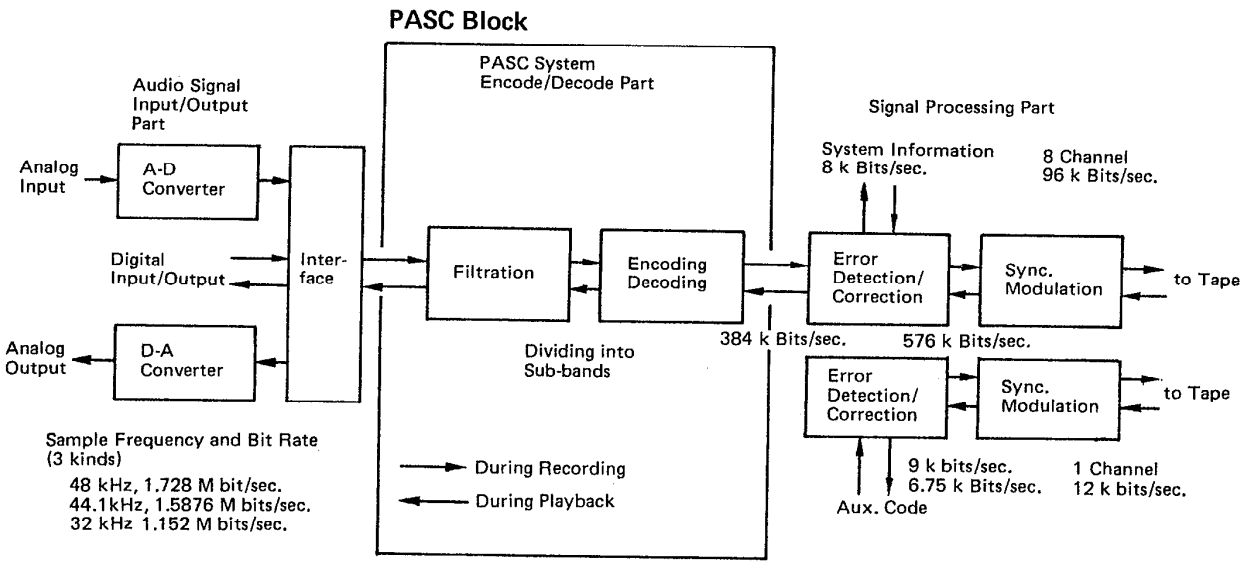


Fig. 8

PASC'S ENCODING ACTIONS

Fig. 3 shows a block diagram of PASC operation during a recording time. Every audio signal is digitalized before entering the PASC.

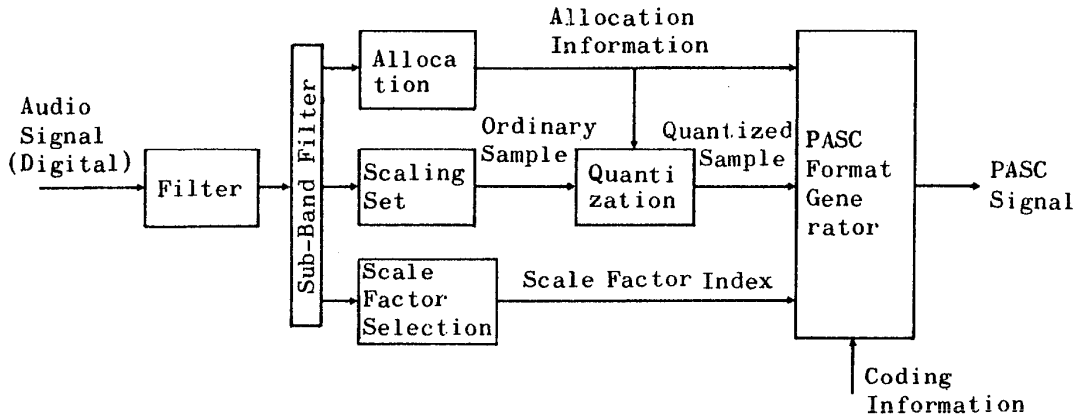
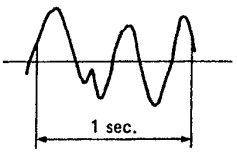


Fig. 9 PASC Encoding Block Diagram

STEP 1. DIVIDING SIGNALS INTO BANDS BY BAND-PASS FILTER

Audio signals, quantized and input, are first divided into 32 bands as they pass through the FIR digital SBF (SBF = Sub-Band Filter).

In the case of sampling frequency 48 kHz, for instance, 48 ÷2 ÷ 32 = 750 Hz forms a BPF band. With signals bearing an audio band between 20 Hz ~ 48 kHz, it can be expressed that audio signals have been divided into 32 sub-bands of 750 Hz. Fig. 10 Shows the pattern analogically.



Signals divided into 32 bands by BPF

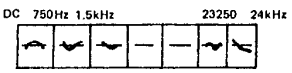


Fig. 10

As mentioned above, audio signals have been digitalized before being filtered actually. Through matrix operation, 32 sub-band signals can be determined continuously. 512 data out of continuous input signals are taken in, operated, and then each 32 audio data are moved and let through filtration.

At the time of filtration, signals on the input side of SBF IC are 16 ~ 18 bit digital signals and those on the output side are 24 bit, more finely quantized than input signals.

The state of operation with regard to the above is pictured to the right.

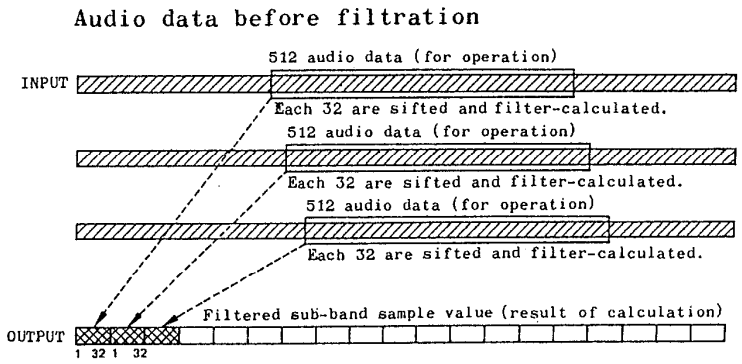

Audio data before filtration
512 audio data (for operation)
INPUT
Each 32 are sifted and filter-calculated.
512 audio data (for operation)
Each 32 are sifted and filter-calculated.
512 audio data (for operation)
Each 32 are sifted and filter-calculated.
Filtered sub-band sample value (result of calculation)
OUTPUT
1 32 1 32

Fig. 11

32 data obtained through operation are drawn up in due order from low to high frequency bands. If lower ones from the lowest are collected in the time-axis direction, 0 ~ 750 Hz band signal data will be obtained. Groups of data having been divided by SBF are arranged by sub-bands, and every time the number of sub-band data comes up to 12, the data are processed as 1 unit. In short, 32 sub-bands × 12 data = 384 data re-processed as a unit.

In the case of 48 kHz sampling frequency, 384 × 1/48,000 = 8 m sec is PASC's signal processing unit time.

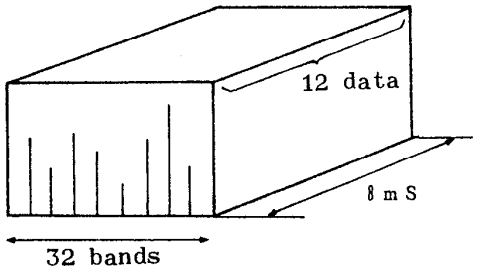


Fig. 12

That is to say, PASC continues to process signals at a rate of 125 times/sec as long as audio signals are supplied.

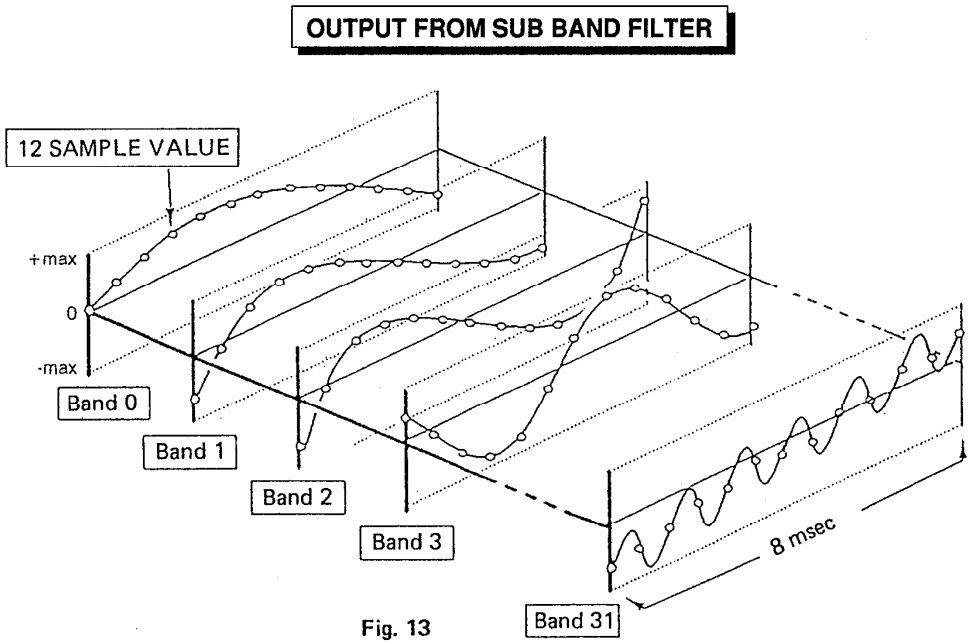
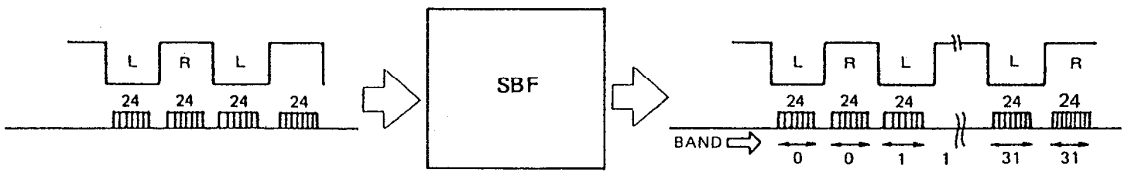


Fig. 13



STEP 2. SUB-BAND SIGNAL SELECTION AND TAPE-RECORDING BITS DESIGNATION

<Determination whether audible or inaudible to human's car>

To determine it, the following masking theory is adopted.

- Human's audible level curve dependant on frequencies
- Masking effect by surrounding noises

Regarding each sub-band in STEP 2,

1. Whether the data is audible to human's year or not (Whether it should be tape-recorded or not), and
2. How many bits when recording.

These are decided immediately and simultaneously.

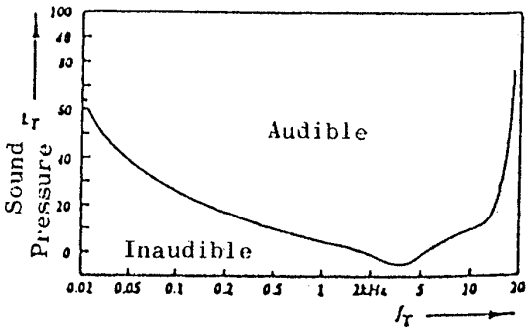


Fig. 14

<Allocation of quantized bits to audible signals>

Output from SBF is 24-bit data as mentioned before. Recording this data as it is does not lead to high-efficiency coding. Thinning it evenly into 10-bit data will result in conspicuous deterioration of sound quality and listeners will recognize it as a strange sound easily.

Since the audio data transfer rate of PASC is 384 k bits/sec (cf. ordinary coding requires 1.536 k bits), limited bits should be apportioned effectively. For this purpose, PASC uses some rules. Typical ones of which are as follows:

(1) Apportionment of bits to suit for human's auditory characteristics, and

(2) Apportionment of bits depending on audible signal level.

In the case of (1), the sub-band covering the frequency to which human's year is sensitive is alloted big quantized bits, and other sub-bands smaller bits, as is manifest from the auditory characteristics shown in Fig. 14.

The borderline curve (hearing threshold) where sound is barely audible or inaudible differs depending on individuals. For PASC, a curve with a margin applicable to very sensitive persons has been set.

In the case of (2), the number of bits is determined in proportion as signal protrudes from the audibility curve shown in Fig. 14.

Exemplified below is how the number of quantized bits is assigned to the same band with a few examples concerning the cases of (1) and (2) above.

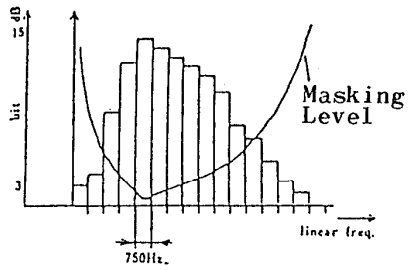


Fig. 15

Fig. 15 shows the case where there are signals evenly over the entire bands. For the smallest, the sample data itself is alloted 2 bits, the entire sub-bands 6 ~ 8 bits, and for the maximum 15 + 6 = 21 bits are assigned to the sub-bands as shown in the drawn pattern. As a matter of course, the lower the barely audible sound pressure of the frequency (at which man's ear is sensitive), the bigger the number of bits assigned.

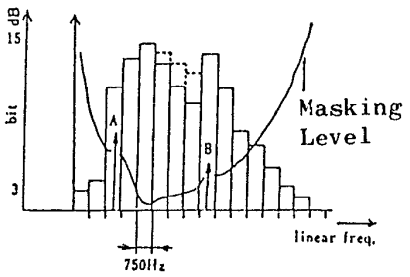


Fig. 16

Fig. 16 shows the case where only A and B are high in sound pressure. Sub-band 2 where sound A is located is alloted 10 or more bits (generally 5 ~ 6 bits). Consequently bits of other sub-bands are cut as shown by broken lines. But this has no influence upon the auditory sense since there has been no sound.

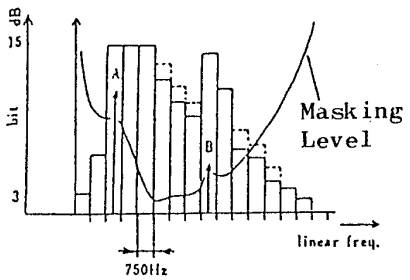


Fig. 17

If the level of A is higher as shown in Fig. 17, PASC assigns 21 bits (the maximum number of bits) to this sub-band.

As explained above, this part of signal processing by PASC has been so designed as to act according to a very flexible logic.

<Allocation Information>

The number of bits alloted to each band is transferred as allocation information by 4-bit binary code to the next stage (SBC). This is an expression with 4 bits through comparison of the peak of each signal with the masking level as shown below.

Allocation Information	
Number of Bits	Allocation Information
0	0000
2	0001
3	0010
4	0011
)	)
15	1110

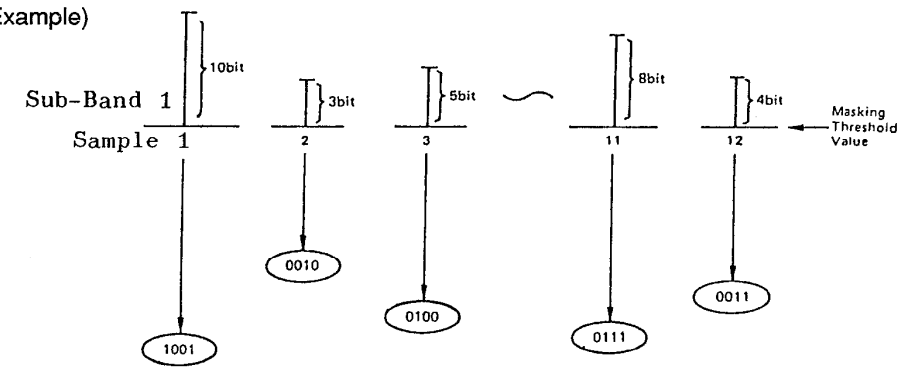
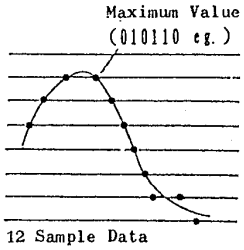


Fig. 18

STEP 3. PASC FORMAT OF AUDIBLE SIGNAL

Through steps 1 and 2, signals to be recorded on the tape have been determined. Next step is to arrange these signals to the PASC format in compliance with the DCC standard. Used for this purpose are IC called SBC (Sub-Band Coding), etc.



This value (the maximum value of each sub-band) is called a 'scale factor.'

Fig. 19

As mentioned above, 12 data are housed in each sub-band. Fig. 19 shows the state as viewed analogically. (Digital data on the practical side)

In the PASC format, the maximum value is detected out of 12 data, and it is quantized by 6 bits for 32 sub-bands evenly.

This maximum value represented by 6 bits is called a 'scale factor.'

In the next place, the 12 data are quantized with the number of bits (one of 2 ~ 15 bits). Fig. 20 shows the state.

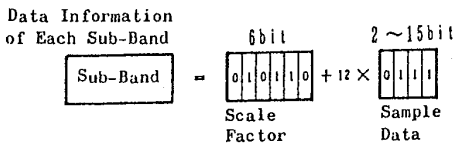


Fig. 20

12 samples × 24 bits = 288 data bits per sub-band. This data, if audible, goes through PASC coding and the number of bits gets between the following minimum and the maximum:

Minimum - 6 + 12 × 2 = 30 bits

Maximum - 6 + 12 × 15 = 186 bits

Actually PASC signal is completed with coding information including (1) sub-band No. ,(2) number of quantized bits of this sub-band, etc added to it. (see Fig. 21)

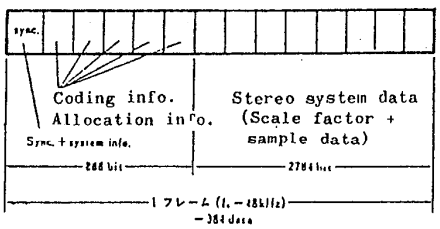


Fig. 21 PASC Data Format

To supplement Step 3, the following explains the meanings of 'scale factor' and each sample data.

<Scale Factor>

Due to quantization over the entire audio bands by use of the same scale, the scale factor determines the dynamic range. In short, the scale factor indicates the ratio of the level of the signals housed in a sub-band to the entire audio signals.

Output Level		Scale Factor	
+5dB	———	000000	
+4dB	———	000001	
+2dB	———	000010	The scale factor is weighted by 2 dB for a 1 bit of change and, therefore, the dynamic range of DCC is 6 bits = 124 dB.
	———		
	———		
	———		
–116dB	———	111101	
–118dB	———	111110	

Fig. 22

<Quantized Bits>

The number of quantized bits given to each sub-band is equivalent to the S/N ratio. If the number of the bits is small, it is detected as a quantized noise depending on frequencies. If it is quantized with maximum 15 bits, $15 \times 6 + 2 = 92$ dB will become the S/N of DCC.

<Scale Factor and Its Relations>

Providing there is a value X = 23487, this value is expressed in the case of PASC as follows: $X = 10^5 \times 0.23487$.

The index of '5' is equivalent to the scale factor, and indicated by 6 bits as '000101.' Depending on the number of quantized bits determined by the sub-band in which the value is housed, the 0.23487 varies, for instance, to become 0.235 or 0.23 as sufficient.

(Example)

For 5-bit expression of X = 23487,

Index part: 000101

Mantissa part: 10111 (= 23)

If the sub-band to which this value belongs is important, it is turned into PASC data by use of 15 bits,

Index part: 000101 (unchanged)

Mantissa part: 101101110111111.

PSC'S DECODING (SIGNAL REGENERATING) ACTIONS

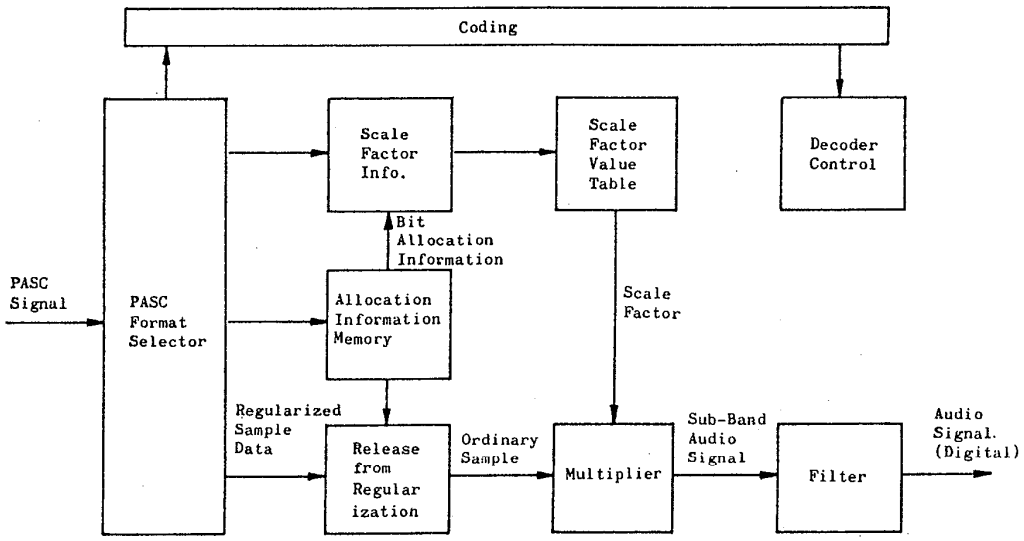


Fig. 23

Fig. 23 is a block diagram showing actions of PASC during decoding.

The flow is fundamentally in reverse order of encoding. Signals read out of the head are waveform-shaped, returned into 8-bit unit data through 10 → 8 demodulation, and then undergoing error-correction, they are returned into PASC format data, that is, they are classified as follows:

- Which sub-band
- Number of scale factors
- Bits at quantization
- Inport of 12 data

The data are returned into 12-point data of maximum 32 batches per 8 ms. At this time, according to coding information or allocation information, the signal wave form of each sub-band is returned into a waveform of correct amplitude by use of scale factor.

Thereafter, these are subjected to multiplication to be signals covering the entire audio bands.

7. Stationary Thin-Film Head Construction

Stationary thin-film head, which excels in integral density, is produced in making products low-priced and uniform in quality. Also, sharp formation of magnetic field and advantageously high saturated magnetic flux density help us improve the recording density greatly.

As compared with the conventional heads, it is less expensive for the number of tracks due to smaller interstices between tracks (narrower guard bands).

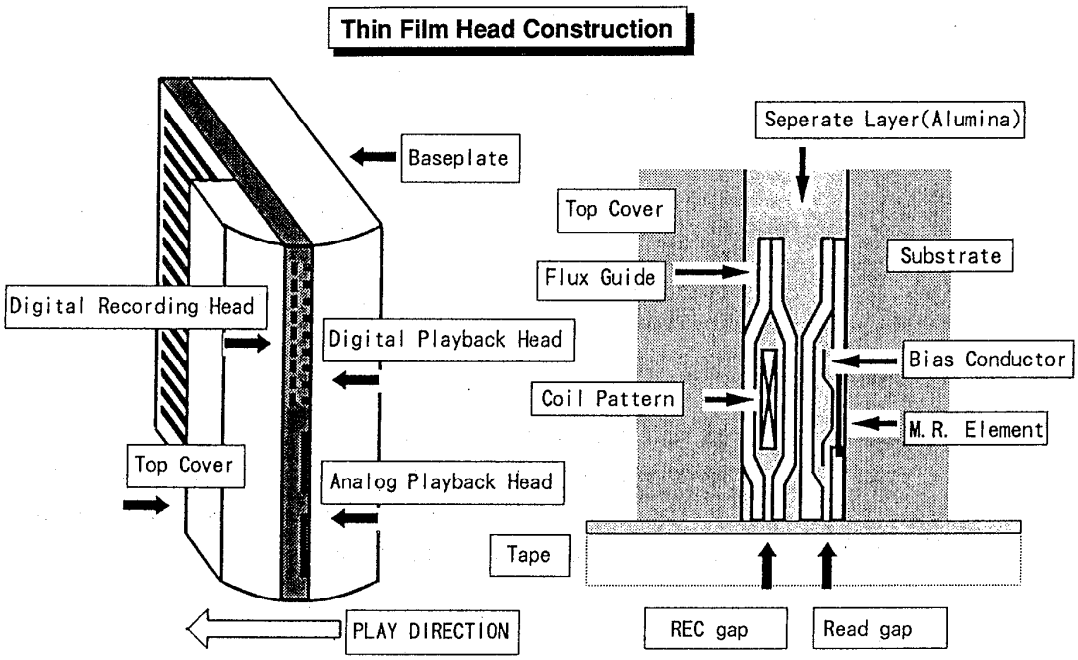


Fig. 24

The DCC system required new type thin-film heads to be designed, and three kinds of heads are combined at present. The recording head used to record digital audio signals has 9 Integrated Recording Heads (IRH) in it. Besides, there are 9 Magneto-Resistive Heads (MRH) used for playback of the digital signals, and 2 Magneto-Resistive Heads (MRH) used for playback of analog audio signals.

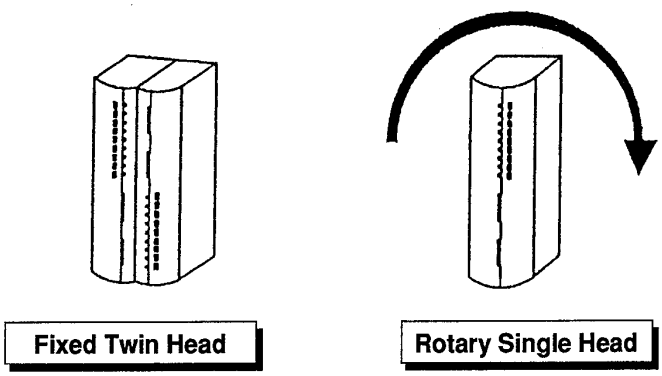


Fig. 25

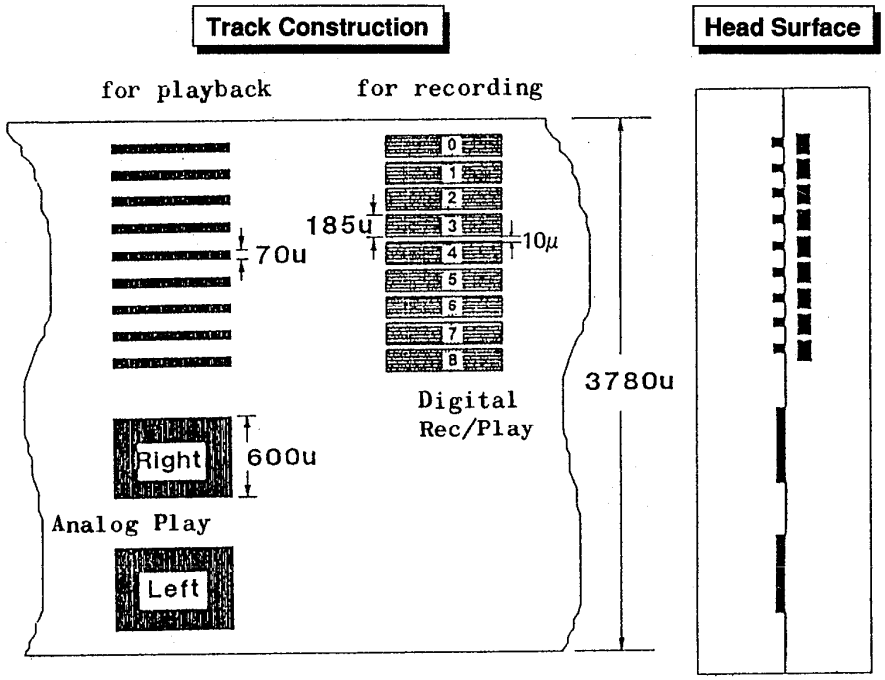


Fig. 26

Digital audio heads are located on one side (half) of the head part, and audio analog heads are on the other side (half).

Therefore, the direction of a DCC tape running in the recording mode is reverse to that of the tape running in a compact cassette during recording.

A portable type DCC uses 2 fixed heads overlaid one on the other but in opposite directions. In the case of a table top DCC and car DCC, a rotary head is used, for selection of either sector A or sector B of the tape used.

Digital signals are recorded on 9 parallel tracks. (Track Pitch = 195 μm, Track Width = 185 μm)

The playback head width is 70 μm. The reason why the head width has been made narrow is that deterioration of playback signals caused by azimuth angular deviation should be minimized even when the head gap is inclined during recording. Deterioration is thus smaller than in the case of a compact cassette.

Comparison with analog cassette

As shown on page 20, DCC's digital signals are on the upper side of sector A of the tape running in the recording/playback mode, whereas ACC's are on the lower side contrary to the conventional concept of sectors A and B.

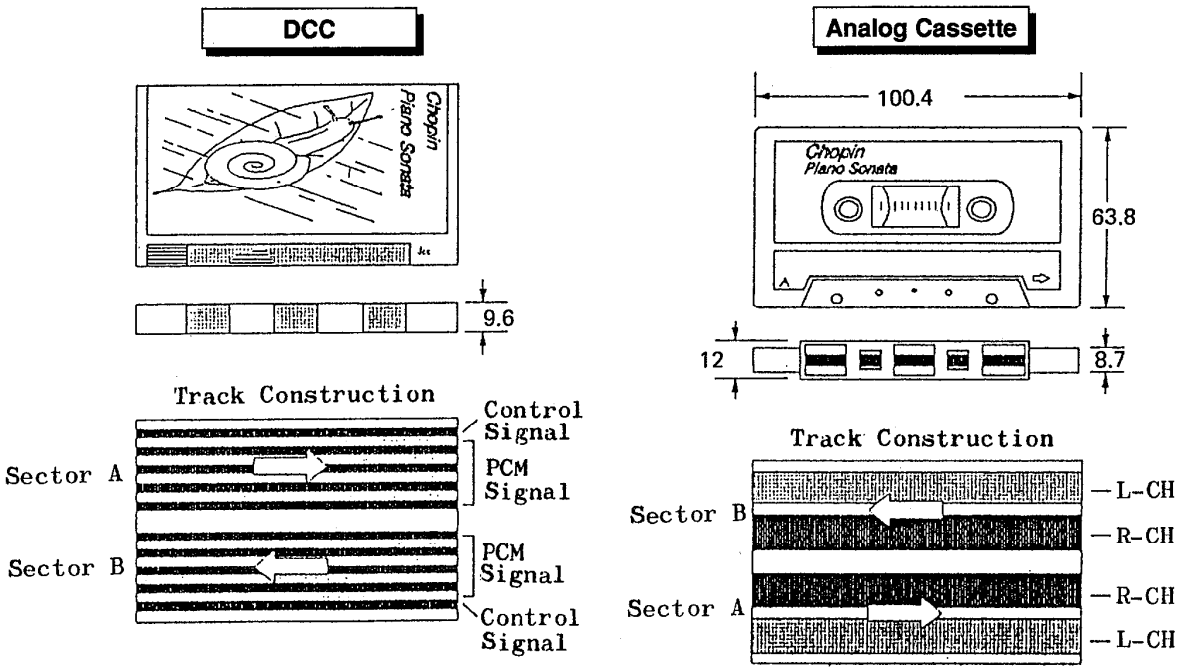

DCC
Chopin
Piano Sonata
9.6
Track Construction
Control
Signal
PCM
Signal
Sector A
Sector B
PCM
Signal
Control
Signal
Analog Cassette
100.4
Chopin
Piano Sonata
63.8
12
8.7
Track Construction
Sector B
L-CH
R-CH
Sector A
R-CH
L-CH

Fig. 27

Head Block Construction

Construction of Mechanism for Table Top DCC

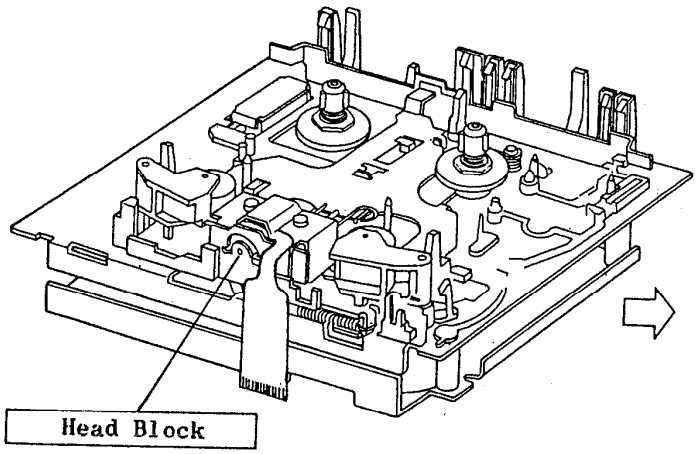


Fig. 28

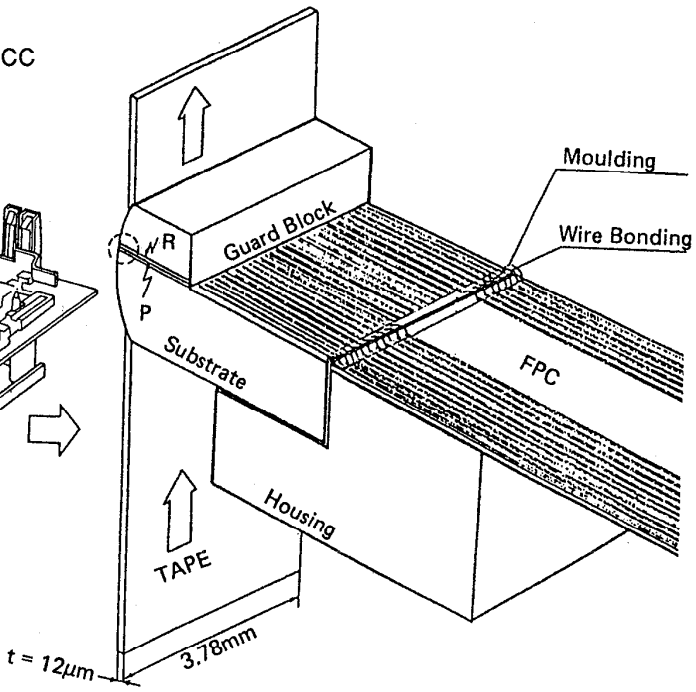


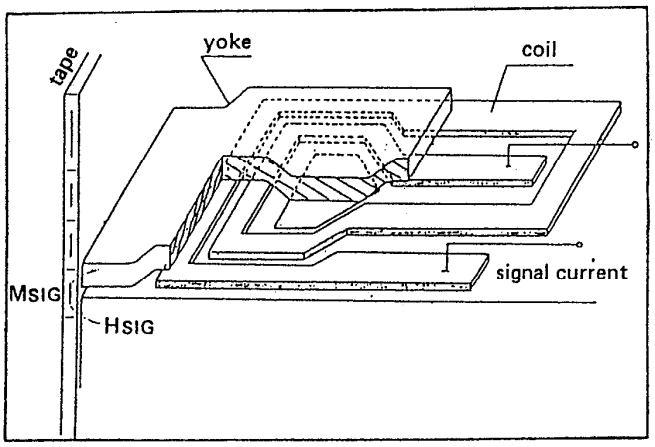
Fig. 29

Rec Head/IRH Head

Recording current of about 0.15A is applied in pulse mode.

Unlike analog, this pulse record is used to reduce recording current.

Shown below are construction of actually used thin-film part, and the state of recording on tape. According to channel bits input, magnetization takes place by inverse characteristics as shown below.



Recording Head

Fig. 30

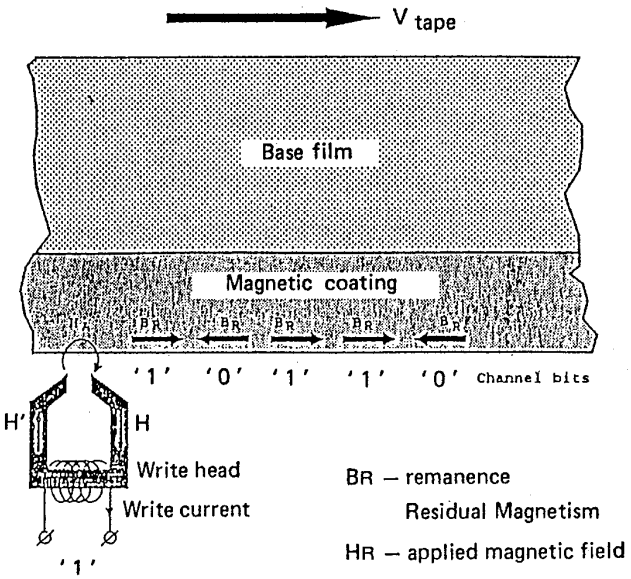


Fig. 31

Playback Head/MR Head

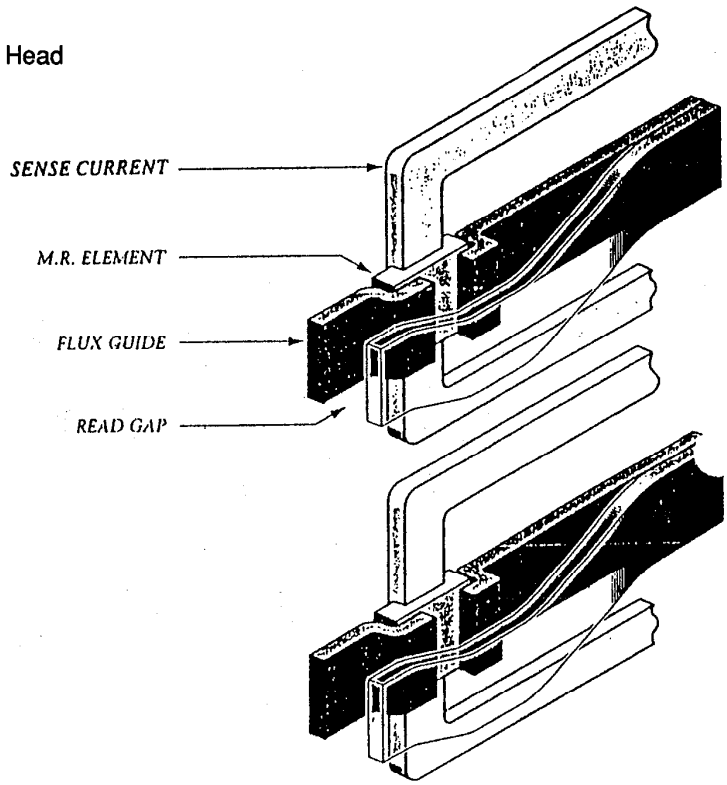


Fig. 32

In an integrated recording head, the signal current conductor is surrounded by a flux guide which concentrates the magnetic field into the recording gap in conventional fashion. The MRH playback head, on the other hand, features an advanced magneto-resistive element whose resistance varies with the magnetic field impressed on it from the tape, via the flux guide. A constant current is fed through the element, so that the voltage across it varies with the magnetic field on the tape.

Magneto-resistive heads are excellent for reading DCC bit transition.

For analogue playback, the high stability and absence of noise and hystereiss of magneto-resistive heads also ensure top quality. At the same time, the inherently high bit rate capability allows for a wide frequency response.

The head face has a thin anti-wear coating; continuous tape travel across the head causes no damage.

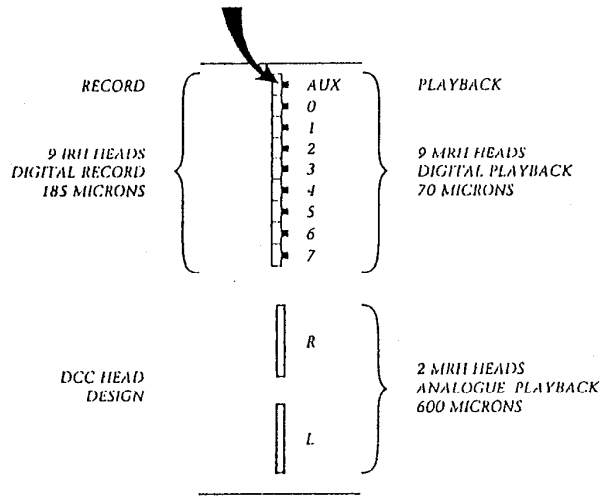


Fig. 33

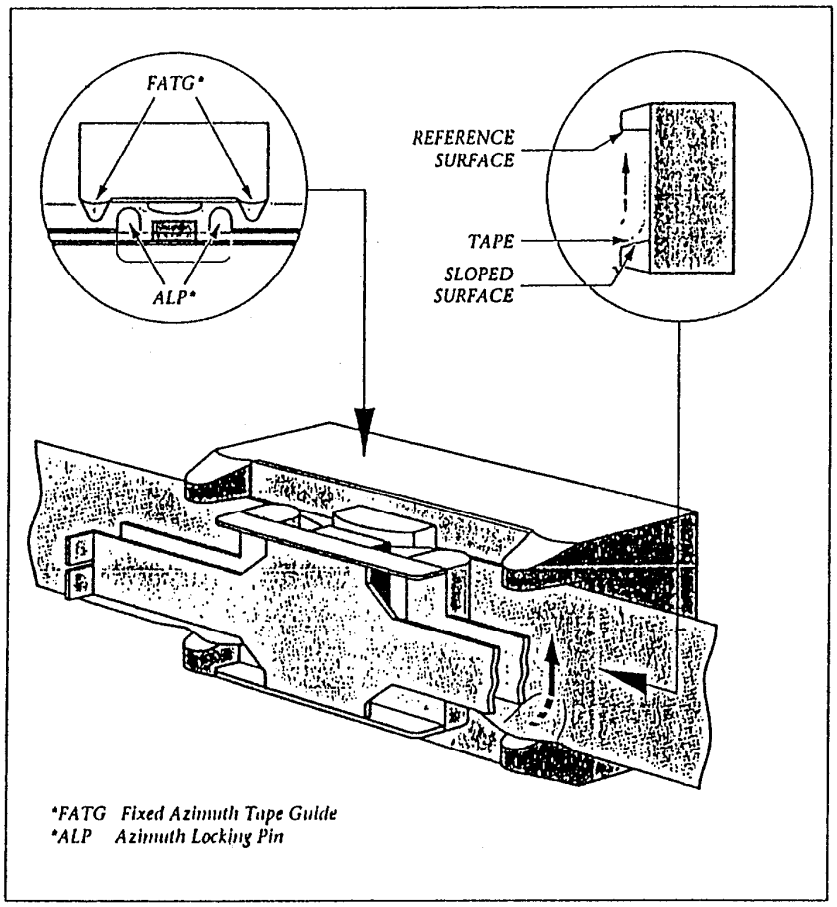
8. DCC Mechanism

One brand-new feature of the DCC cassette is the two Azimuth Locking Pins (ALPs). In conjunction with the Fixed Azimuth Tape Guidance (FATG) mechanism fitted to the head assembly, the ALPs ensure not only improved tape-head contact, but also consistently repeatable alignment of the tracks on the tape with the heads.

The ALPs increase the wrap-around angle of the tape against the head. This extends the tape-head contact area and optimizes the physical conditions for signal recording and reading. The tape is also stiffened in this crucial tape guidance area, and this contributes to the high accuracy of the FATG mechanism.

In the FATG mechanism, special slots are mounted on either side of the head assembly. The two top edges of the slots form reference surfaces to align the tape with the head. Meanwhile, the sloping profiles of the lower parts of the slots gently force the stiffened tape upwards against both reference surfaces. For all practical purposes, this simple device eliminates azimuth error.

The ALPs/FATG design requires no complicated mechanisms or close tolerances. Its very simplicity ensures permanently accurate tape-head alignment.



Tape-head engagement: optimal wrap-around with the ALPs (inset) and azimuth alignment with the FATG (inset)

Fig. 34

9. DCC Cassette Tape

The DCC cassette is a Compact Cassette with a diffenence. It has the same basic dimensions, records on forward and reverse tracks, and uses (video) chrome or equivalent tape. Modern technology, however, has produced a much improved design. Both the new cassette and its holder are more stylish and more convenient.

The cassette body is also made thinner overall, because the record/playback head is more compact.

New materials are used in the DCC cassette itself. They are specified for use over a wider temperature range than the Compact Cassette.

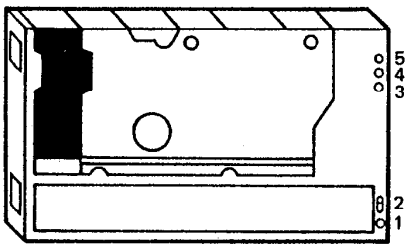
The normally exposed tape, and the tape drive wheels, are covered by a slider. This provides the tape with built-in protection against soiling and scratches. It also locks the tape reels to solve an old problem of the cassette medium; in a DCC cassette there is little chance for the tape to unwind, get into a tangle, and then become jammed. When the cassette is loaded, the slider is automatically pushed aside. Thanks to this device, cassettes can safely be carried around without their houlders. So not only is the cassette more attractive vicually, it is also easier to pick up and use in all applications and it takes up less storage space.

The length of a blank DCC cassette can be indicated by holes in the rear of the housing.

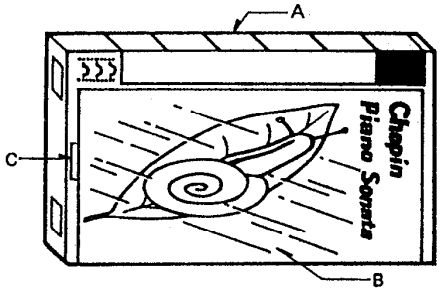
These enable DCC decks to calculate and display the remaining recording time.

Accidental overwriting can be prevented by a record protection switch.

DCC Blank Tape



DCC MUSIC TAPE



A : Slider for tape protection
B : Label
C : Hole for Automatic Loading

Purpose of each hole

HOLE

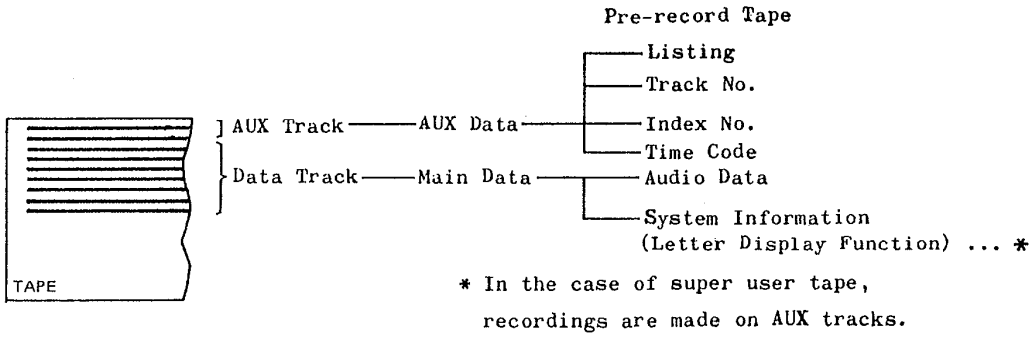
1. Detection of DCC/ACC
2. Protection of error erace.
3. Tape Playing Times (Min.)
4. Tape Playing Times (Min.)
5. Tape Playing Times (Min.)

	45	60	75	90	105	120	U
3	●		●		●		●
4	●	●			●	●	
5	●	●	●	●			

● = hole present U = undefined

Tape playing times.

10. Tape Format



1) Main Data Format

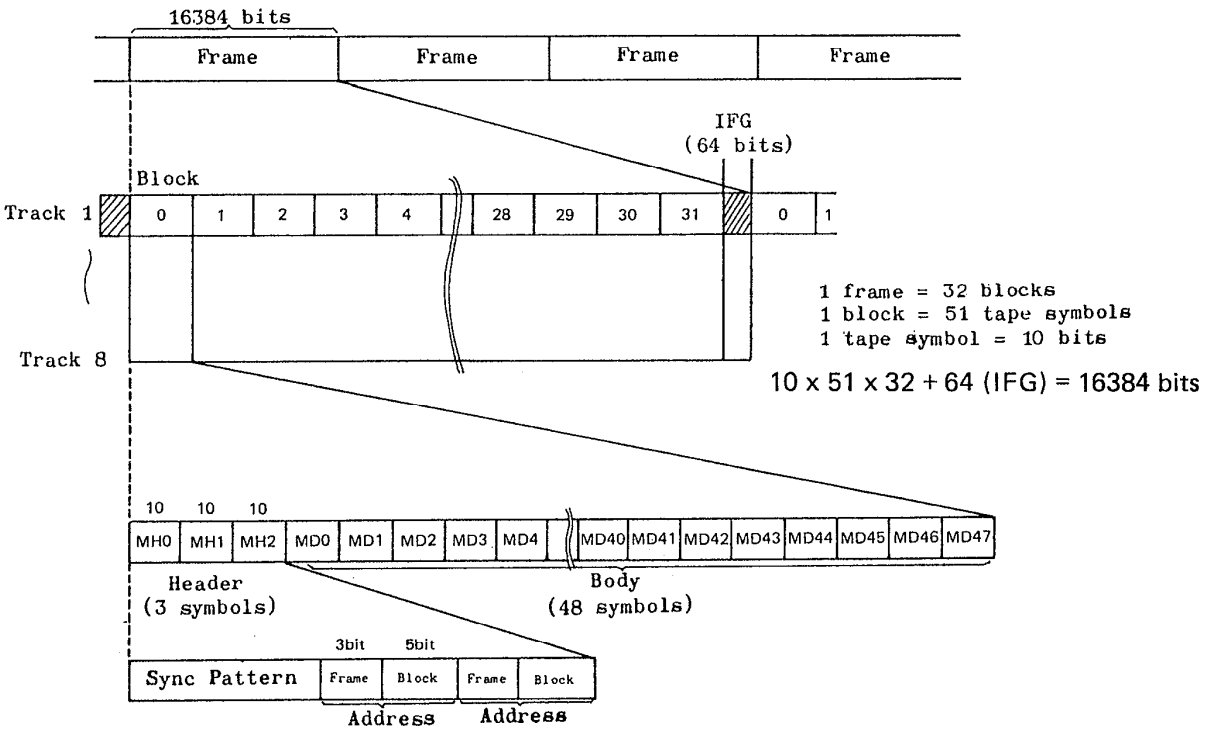
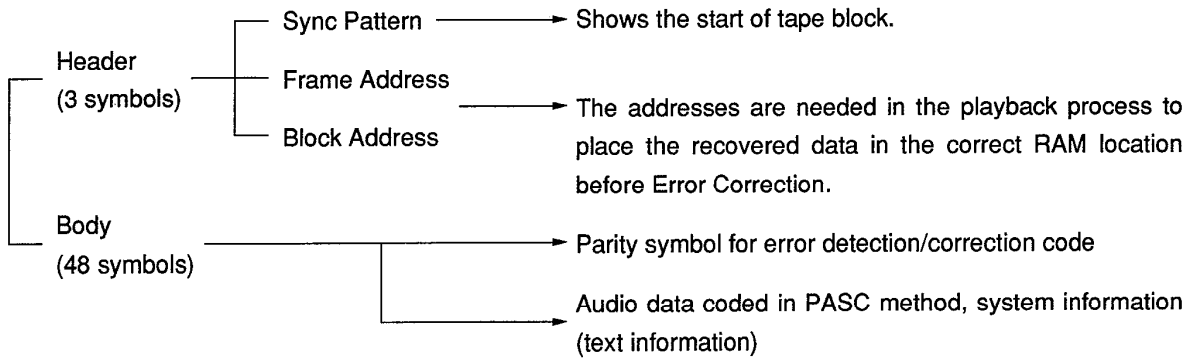


Fig. 35


Header
(3 symbols)
Sync Pattern
Shows the start of tape block.
Frame Address
Block Address
The addresses are needed in the playback process to place the recovered data in the correct RAM location before Error Correction.
Body
(48 symbols)
Parity symbol for error detection/correction code
Audio data coded in PASC method, system information (text information)

- IFG (Inter-Frame Gap)

The signals recorded on tape can be divided into Tape Frames. Between Tape Frames an Inter Frame Gap (IFG) with variable length is provided, to accomodate for small deviations (such as clock jitter) from the sampling frequency used during recording. Its nominal length is 64 bit periods, corresponding to about 0.4% of the nominal Tape Frame length (including IFG) of 16384 bit periods. The IFG carries a signal that has alternating polarity at every bit position.

2) AUX Data Format

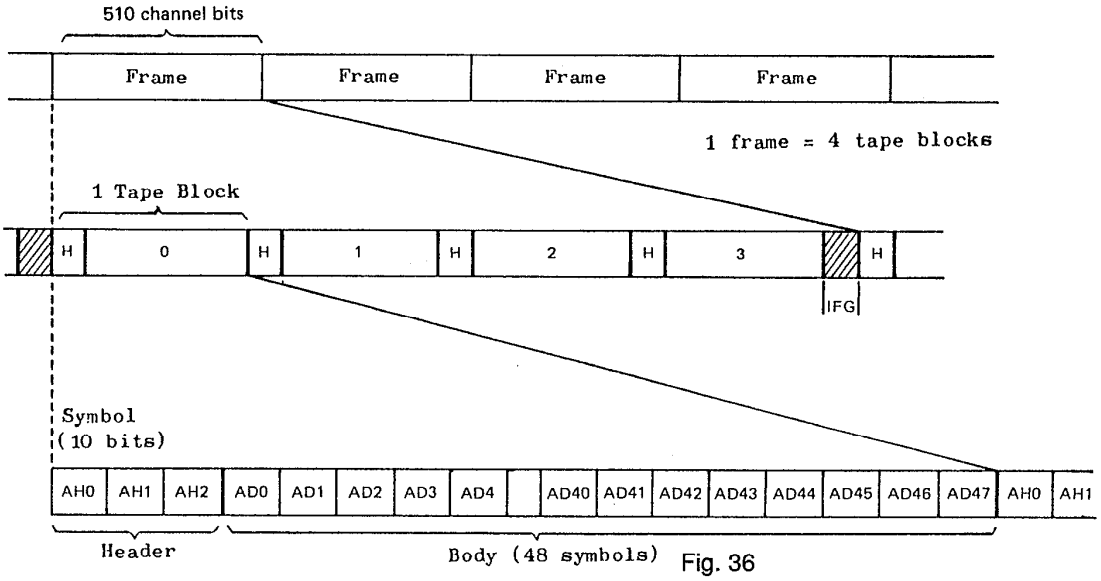
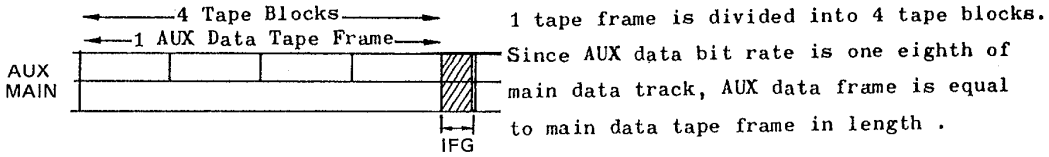
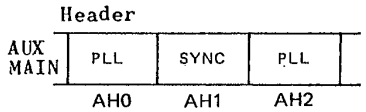


Fig. 36


4 Tape Blocks
1 AUX Data Tape Frame
AUX
MAIN
IFG
1 tape frame is divided into 4 tape blocks.
Since AUX data bit rate is one eighth of
main data track, AUX data frame is equal
to main data tape frame in length .



Header contains two 10-bit PLL sequence (AH0 and AH2) to enable easy clock recovery. They also indicate whether or not the body is recorded.

Body Body information is repeated in each of 4 tape blocks of tape frame, and includes information given below.

AD	MSB 7	6	5	4	3	2	1	LSB 0
0	0	0	0	0	CONTROL INFO			
1	MARKER INFO							
2	TRACK NUMBER							
3	INDEX NO. / CHAPTER NO.							
4	SCT	ABS.FRAME			SOB	ABS.HOUR units		
5	ABS MIN.tens				ABS.MIN.units			
6	ABS SEC tens				ABS.SEC units			
7	PAU	TR.FRAME			RES	TR.HOUR units		
8	TR.MIN.tens				TR.MIN.units			
9	TR.SEC.tens				TR.SEC.units			
10	first TOC ITEM							
11	,,							
12	,,							
13	,,							
14	,,							
15	second TOC ITEM							
16	,,							
17	,,							

18	,,
19	,,
20	ADDITIONAL INFO SPECIFIER
21	
22	
23	
24	
25	
26	
27	
28	
29	
30	
31	
32	
33	
34	
35	

3) PASC Frame Format

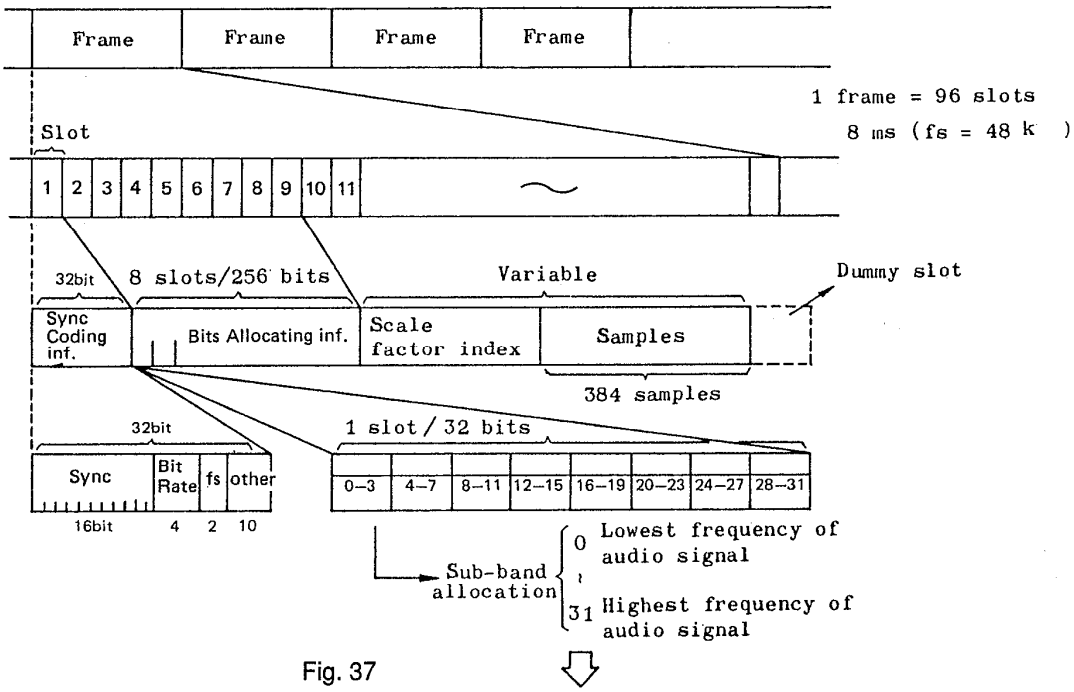


Fig. 37

Scale factor index

For every subband where samples are transfered, a scale factor index must be transfered.

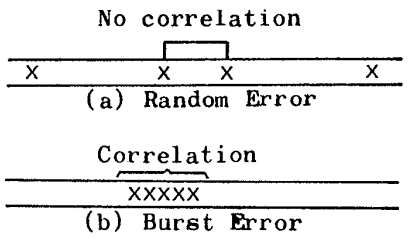
Slot 10	0–5	6–11	12–17	18–23	24–29	30–31
	L–0	R–0	R–1	L–2	L–3	R–3
Slot 11	0–3	4–9	10–15	16–21	22–27	28–31
	R–3	L–4	R–4	L–5	R–5	L–6
Slot 12	0–1	2–7	8–13	14–19	20–25	26–31
	L–6	R–6	L–7	R–7	L–8	L–9

In stereo mode the allocation units must be sent in the following order:

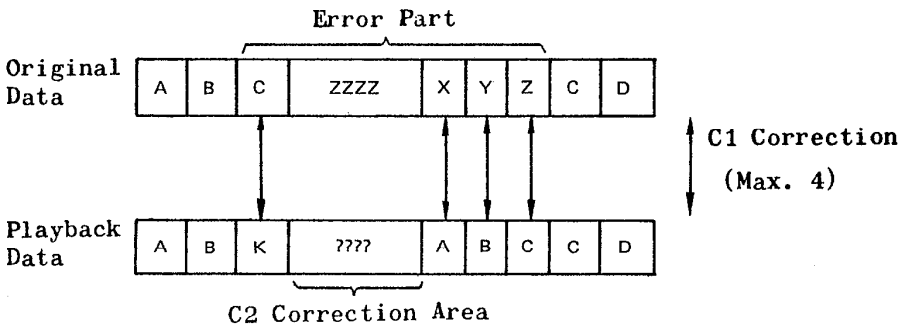
Slot 2:	0..3 L-0	4..7 R-0	8..11 L-1	12..15 R-1	16..19 L-2	20..23 R-2	24..27 L-3	28..31 R-3
Slot 3:	0..3 L-4	4..7 R-4	8..11 L-5	12..15 R-5	16..19 L-6	20..23 R-6	24..27 L-7	28..31 R-7
Slot 4:	0..3 L-8	4..7 R-8	8..11 L-9	12..15 R-9	16..19 L-10	20..23 R-10	24..27 L-11	28..31 R-11
Slot 5:	0..3 L-12	4..7 R-12	8..11 L-13	12..15 R-13	16..19 L-14	20..23 R-14	24..27 L-15	28..31 R-15
Slot 6:	0..3 L-16	4..7 R-16	8..11 L-17	12..15 R-17	16..19 L-18	20..23 R-18	24..27 L-19	28..31 R-19
Slot 7:	0..3 L-20	4..7 R-20	8..11 L-21	12..15 R-21	16..19 L-22	20..23 R-22	24..27 L-23	28..31 R-23
Slot 8:	0..3 L-24	4..7 R-24	8..11 L-25	12..15 R-25	16..19 L-26	20..23 R-26	24..27 L-27	28..31 R-27
Slot 9:	0..3 L-28	4..7 R-28	8..11 L-29	12..15 R-29	16..19 L-30	20..23 R-30	24..27 L-31	28..31 R-31

11. DCC Error Correction

Errors, roughly classified, are random errors (caused mainly by noise component contained in signal) and burst errors (occurring continuously from defect or scars of tape or caused by failure of synchronism).



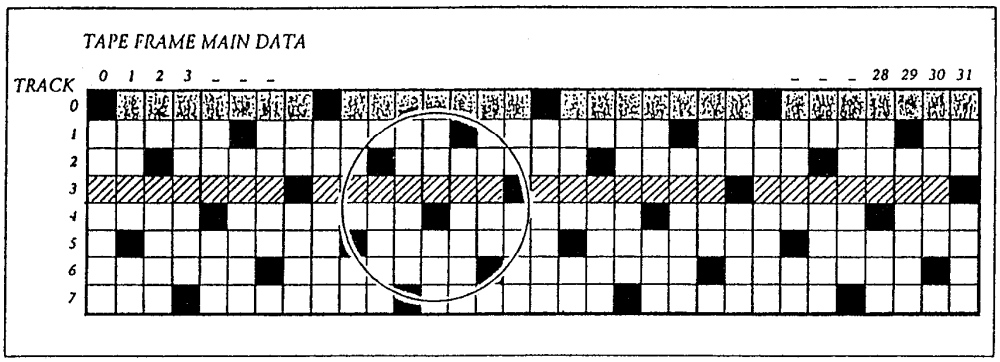
Random Error and Burst Error



A Cross Interleaved Reed Solomon Code is employed to protect the data against random and burst errors. During playback a first code (called C1) is evaluated to detect and - if possible - correct errors within a Tape Block. As the C1 code may correct at maximum 4 error symbols per Tape Block, any errors that can Cannot be corrected are passed to the second (called C2) correction phase as erasures : indicating the location of the erroneous symbol, but not the error value.

At maximum the C2 code can correct 6 of these erasure symbols per code word. The distribution of the symbols for a C2 code word is such that an almost optimum physical distance between the symbols is achieved, resulting in a "chequer-board" pattern. This enables correction of drop outs with a diameter of up to 1.45 mm. The system can even operate if a complete track is missing, although in this case a long drop out in the other tracks is more likely to cause audible sound degradation.

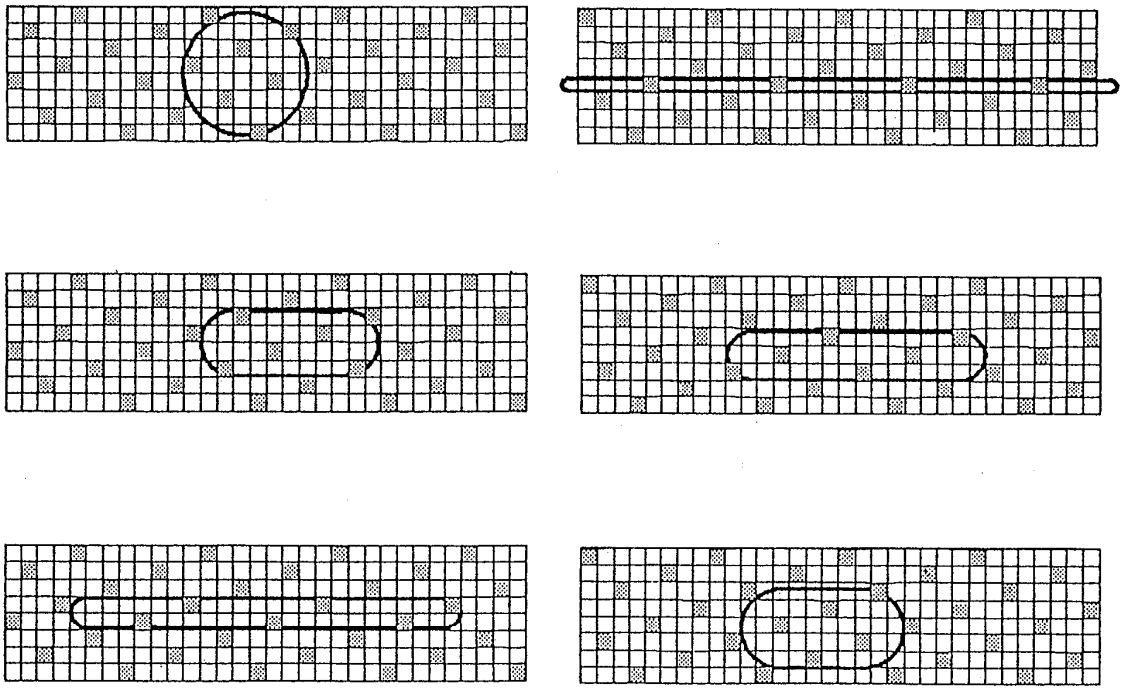
The PASC bytes are distributed onto the tracks in such a way that any failure of the error correction system does not disrupt consecutive PASC bytes: an uncorrectable C1 or C2 code word will not result into a burst error in the PASC signal. This helps the PASC processor to conceal these errors.



PASC data bytes in chequer-board pattern in a tape frame. Adrop out as large as the outline shown does not impair sound quality, nor does the absence of a complete track.

Fig. 38

The area enclosed by 6 C2 symbols in the drawing can be corrected.



Lost part in the area enclosed by 6 C2 symbols in the drawing can be corrected.

12. DCC vs. DAT/CD Format, and Performance Comparison

DCC			R–DAT	CD
Number of Channels		Stereo (2 channels)	←	←
Frequency Range	fs = 48 kHz fs = 44.1 kHz fs = 32 kHz	8 ~ 22,000 Hz 5 ~ 20,000 Hz 5 ~ 14,500 Hz	←	20 ~ 20000 Hz
Dynamic Range		>105 dB	90 ~ 94 dB	>90 dB
THD (+N)		<0.0025%	<0.05%	0.0022%
Wow & Flutter		Crystal Oscillator Accuracy	←	←
<Signal Format>				
Sampling Frequeny		48, 44.1, 32 kHz	48, 44.1, 32 kHz	44.1 kHz
Coding		PASC	—	—
Audio Bit Rate		384 k bits/s	2.46 Mbit/s	2.0338 Mbit/s
Error Correction Method		C1, C2 Reed Solomon	C1, C2 Reed Solomon	C1, C2 Reed Solomon
Modulation Method		8–10 Modulation (ETM)	8–10 Modulation (ETM)	8–14 Modulation (EFM)
Preemphasis		Option	←	←
<Cassette>				
Recording Time		D90: 45 × 2 = 90 min. D120: 60 × 2 = 120 min.	120 min.	60 min. ~ (Disc)
Tape		Cr Tape	Metal Tape	—
Tape Width		3.78 mm	3.81 mm	—
Tape Speed		4.76 cm/s	0.815 cm/s	1.2 ~ 1.4 m/s (CLV/Disc)
Number of Tracks		8 Digital Audio 1 AUX Cord	Helical Scan Method	—
Track Width		185 μm	2.613 mm	0.5 μm (pit)
Track Pitch		195 μm	13.591 μm	1.6 μm

EXPLANATION OF MECHANISM

1. Mechanism Layout

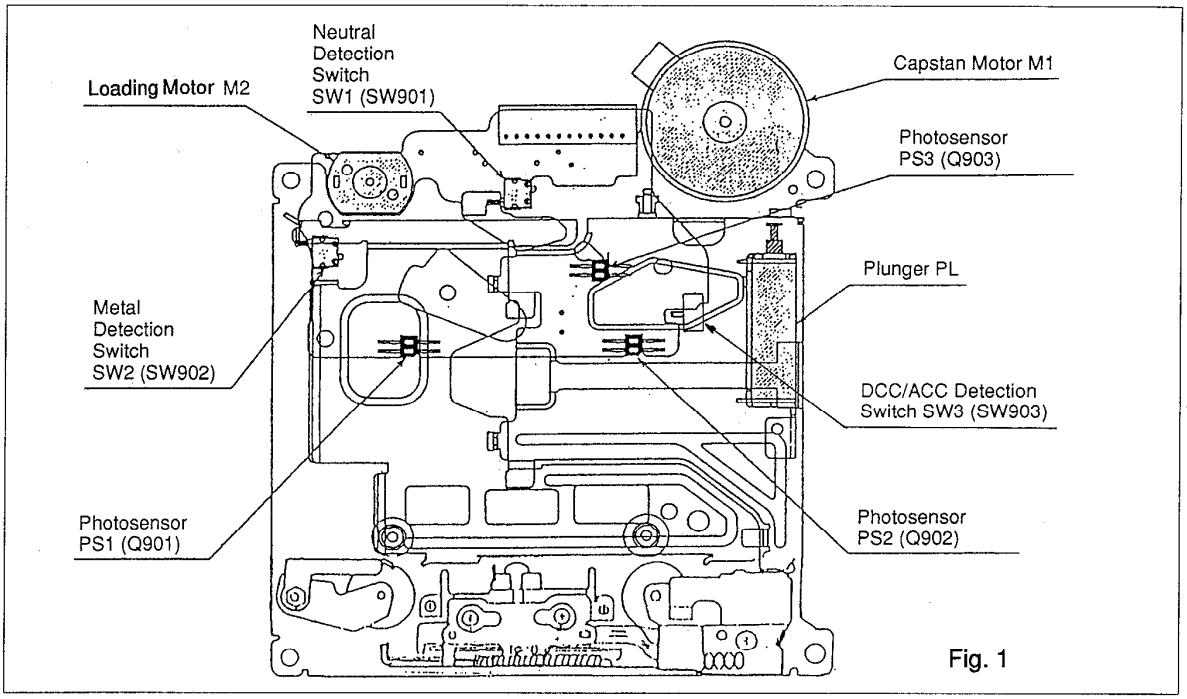


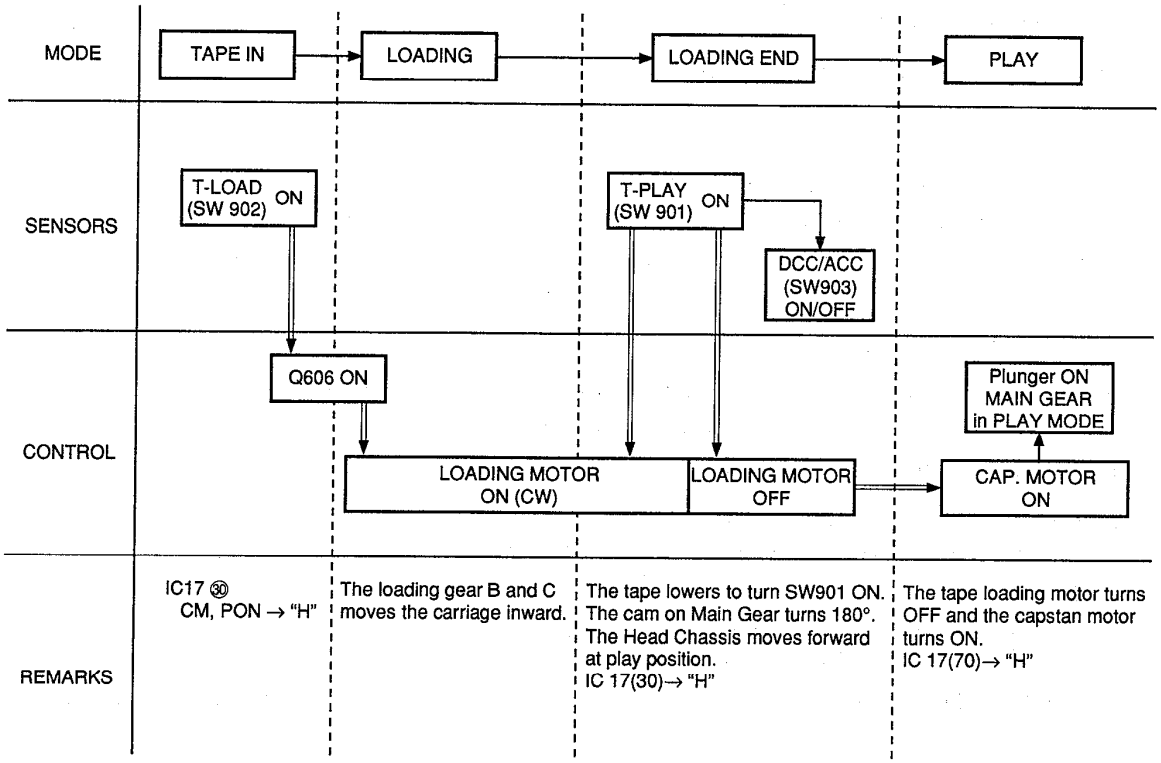
Fig. 1

Functions of actuators and sensors

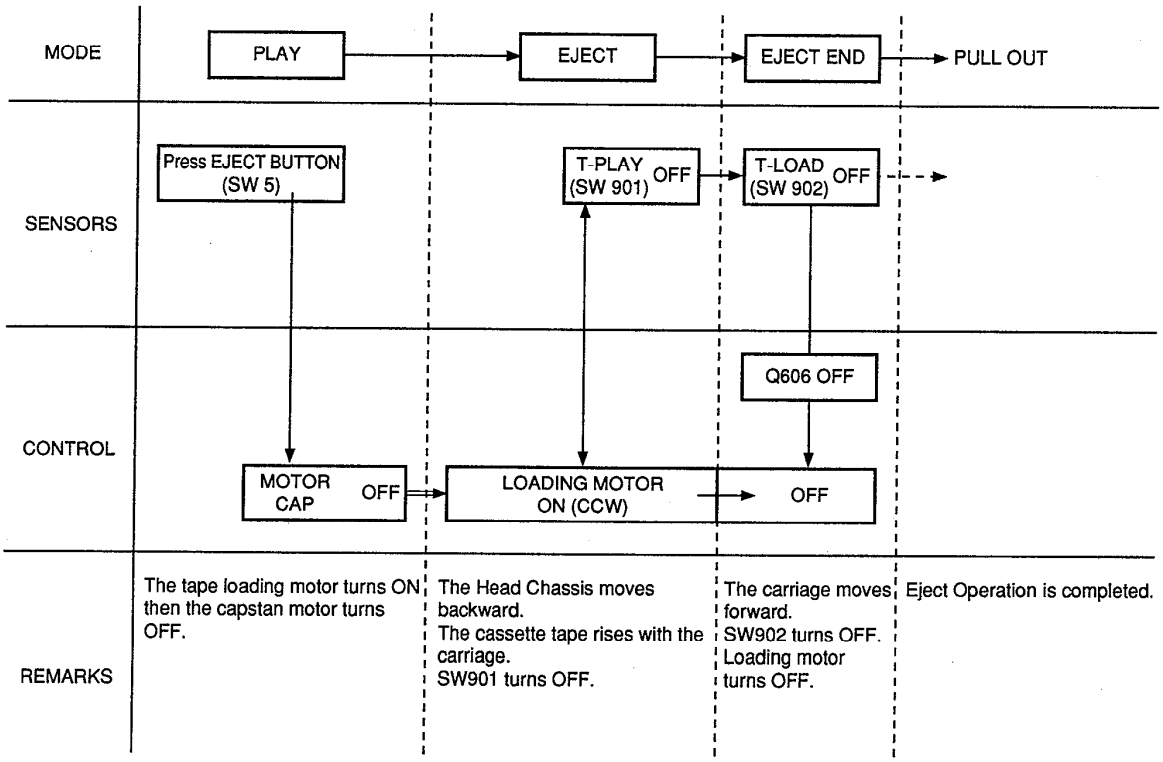
Symbol (No. in PCB)	Part Name	Function
M1	Capstan Motor	1) Capstan and reel table rotation 2) Mode change drive source
M2	Loading Motor	1) Cassette tape loading and ejection 2) FF, Rew (incl. TPS) selection
PL	Plunger	1) Trigger for mode change 2) Fwd/Rev play direction change
PS1 (Q901)	R-side reel table rotation detecting photosensor	1) Detection of R-side reel table rotation and rotating speed
PS2 (Q902)	F-side reel table rotation detecting photosensor	1) Detection of F-side reel table rotation and rotating speed
PS3 (Q903)	Main gear position detecting photosensor	1) Change of mode through detection of main gear stop position
SW1 (SW901)	Neutral detection switch	1) Detection of sub-gear position for FF/REW change 2) Detection of end of loading or of ejecting action
SW2 (SW902)	Metal detection switch	1) Normal/Metal tape discrimination 2) Detection of start of tape loading
SW3 (SW903)	DCC/ACC detection switch	1) Detection of DCC/ACC 2) ACC tape ..... H DCC tape L

2. Loading/Eject Operation

(1) LOADING OPERATION


MODE
TAPE IN
LOADING
LOADING END
PLAY
SENSORS
T-LOAD (SW 902) ON
T-PLAY (SW 901) ON
DCC/ACC (SW903) ON/OFF
CONTROL
Q606 ON
LOADING MOTOR ON (CW)
LOADING MOTOR OFF
Plunger ON MAIN GEAR in PLAY MODE
CAP. MOTOR ON
REMARKS
IC17 ㉚ CM, PON → "H"
The loading gear B and C moves the carriage inward.
The tape lowers to turn SW901 ON. The cam on Main Gear turns 180°. The Head Chassis moves forward at play position. IC 17(30)→ "H"
The tape loading motor turns OFF and the capstan motor turns ON. IC 17(70)→ "H"

(2) EJECT OPERATION



3. Explanation of Each Mechanism

1. Mode Change Mechanism (Main Gear Rotating Mechanism)

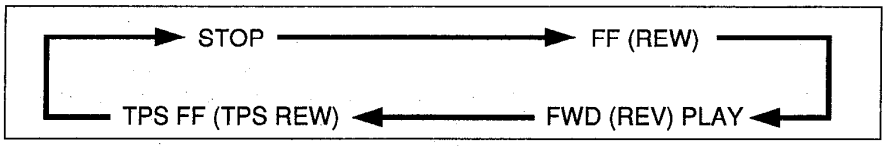
1–1. Functions of main gear

The main gear has the following functions:

1. Change of mode
2. In-Out movements of head baseplate
3. Rotation of playback head
4. Change of power motor drive force transfer route

1–1–1. Change of mode (see Fig. 2)

There are four notches along the outer circumference of the main gear. When pawl B of gear A lever comes to one of the notches, the main gear stops rotation. The four notches are called Mode stations. As the main gear rotates, the mode station changes in the following order repeatedly.



PS3 is used to detect the main gear's position. This sensor turns ON at the STOP position only. (see Fig. 1)

Explanation of movements

(1) When plunger PL is set to ON during rotation of capstan motor M1, gear A meshes with the gear of the pulley on the capstan motor M1 to rotate the main gear.

(2) Even though plunger PL turns OFF, gear A lever's pawl B remains on part C of the main gear, so that the pulley gear is kept in mesh with gear A to rotate the main gear up to the next Mode station.

(3) Upon arrival at the mode station, the gears are disengaged and the main gear stops.

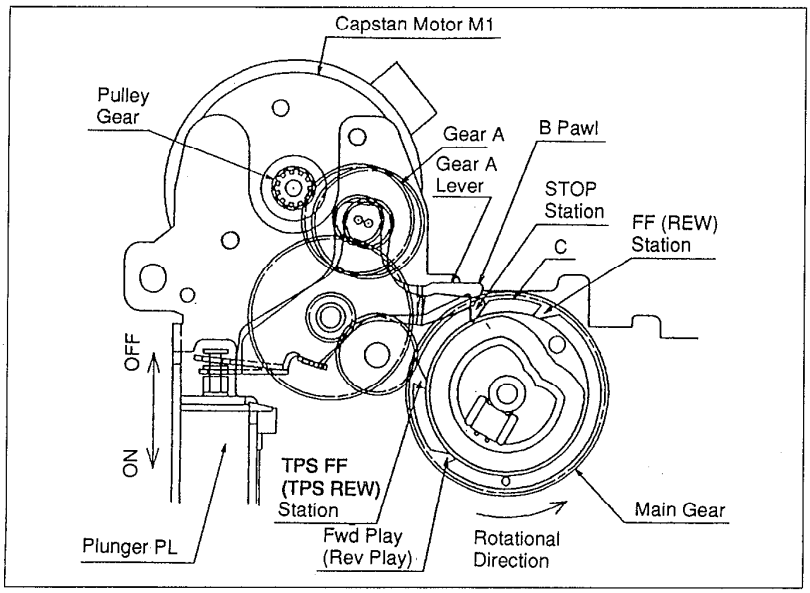


Fig. 2 Main gear's mode change mechanism

1–1–2. In-Out movements of head baseplate

The main gear's cam meshing with the pin mounted to the head baseplate, one rotation of the main gear causes the head baseplate to move In-Out once. (see Fig. 3)

1–1–3. Rotation of playback head

The main gear's cam, turning the Fwd/Rev change lever, causes the rotary mechanism of the head to move. (For detail, refer to Section of 'Fwd/Rev Play Change Mechanism.') (see Fig. 4)

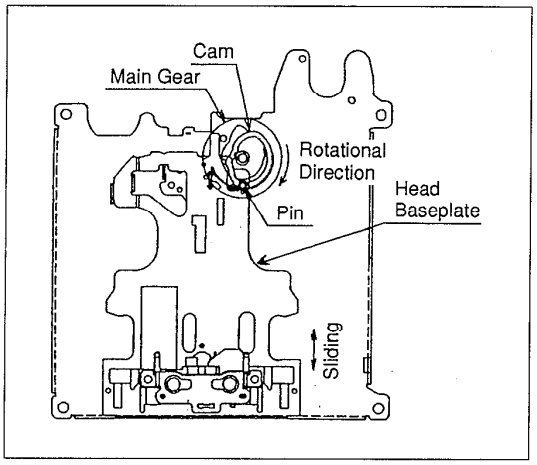


Fig. 3 In-Out movements of head baseplate

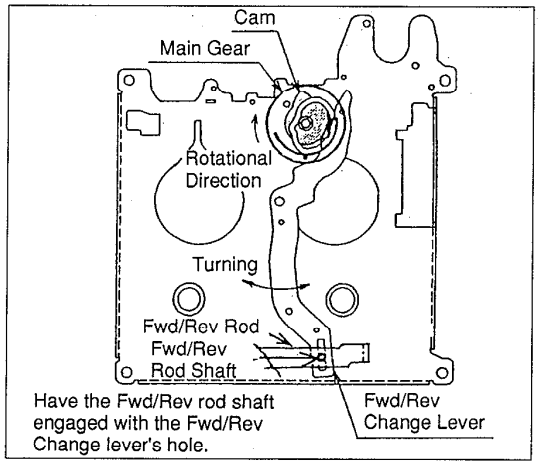


Fig. 4 Rotation of playback head

1–1–4. Change of power motor drive force transfer route

The main gear's cam, turning the LF change lever to move the LF select gear, changes the LF Select gear position to mesh between gear B and gear D. (see Fig. 5) There are two routes as follows:

(1)	Cassette in/out gear series	Load gear B mode (Station . . . STOP)
(2)	FF/REW change sub gear series	Gear D mode (Station . . . FF (REW), FWD (REV) PLAY, TPS FF (TPS REW))

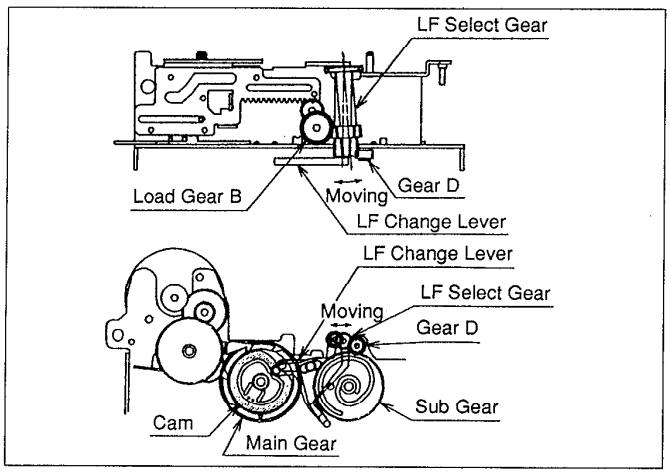


Fig. 5 Change of power motor drive force transfer route

2. FF/REW Mechanism

When the main gear is positioned at FF (REW) or TPS FF (TPS REW) station, the LF select gear is engaged with gear D. Then the sub gear is rotated by the power motor through gear D. (see Fig. 5)

As shown in Fig. 6, the sub gear has a spiral-shaped cam, which turns the FF lever to make the FF gear mesh with the Fwd reel table gear and Fwd flywheel gear or with the Rev reel table gear and Rev flywheel gear, thereby placing the unit into the FF or REW mode.

A, B, and C (shown in Fig. 6) of the sub gear cam are NEUTRAL, FF, and REW positions respectively.

Neutral detection switch SW1 (SW901) is used for detection of the sub-gear position. This switch turns OFF only when the position is NEUTRAL. (see Fig. 1)

For FF or REW, time required for turning the cam from the NEUTRAL position is about 150 ms in either direction from when the switch is turned ON.

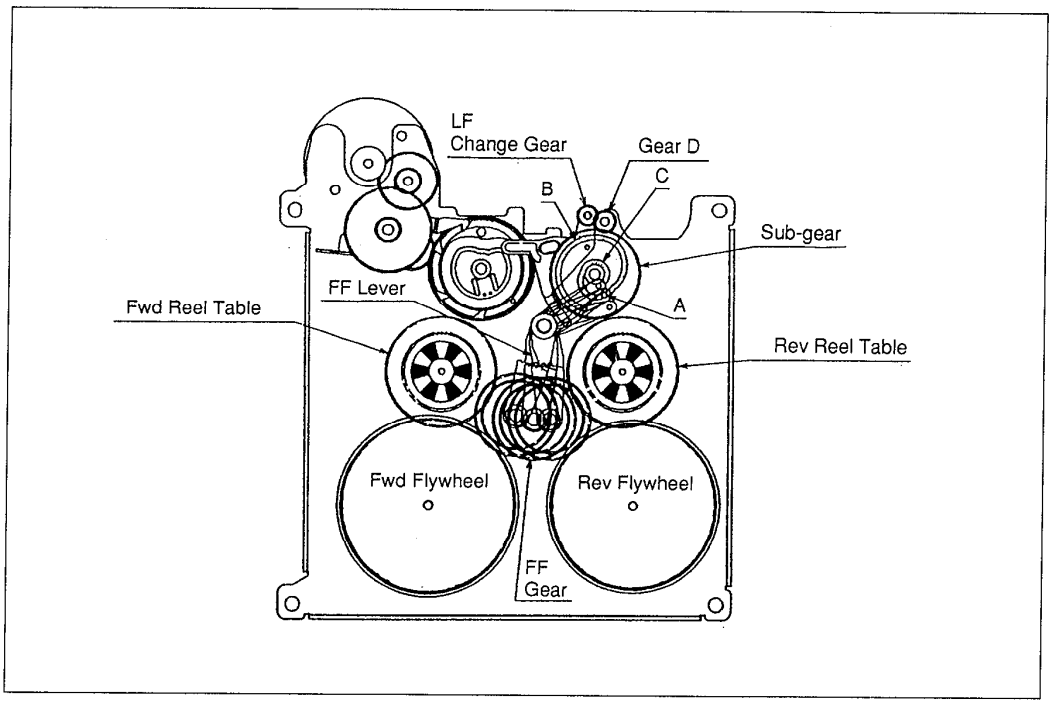


Fig. 6 FF/REW Mechanism

3. Fwd/Rev Play Change Mechanism

While the main gear is rotating from the FF (REW) position to the PLAY position, the Fwd/Rev play direction is to be changed.

3–1. Fwd/Rev change lever movement

(1) On the way from the FF (REW) mode station to the PLAY mode station the main gear causes the A-part of the cam to move the guide part D of the Fwd/Rev change lever to the right. (see Fig. 7)

(2) If the plunger PL is at OFF position, the main control lever is at CCW-turned position. This lever is positioned according to ON-OFF of the plunger. At this time, the main control lever's pawl part E engages with the Fwd/Rev change lever's end part F. When the main gear rotates further, the Fwd/Rev change lever's guide part D moves toward the B direction of the cam. (FF)

(3) In relation to (1) above, if the plunger is at ON position, the main control lever's pawl part E will not get engage with the Fwd/Rev change lever's end part F. When the main gear rotates further, the Fwd/Rev change lever's guide part D moves toward the C direction. (REW)

- Thus immediately after the Fwd/Rev change lever's guide part D passes the A-part of the main gear cam, the Fwd/Rev change lever changes in position according to ON-OFF of the plunger, so the unit is placed into the Fwd or Rev play mode.

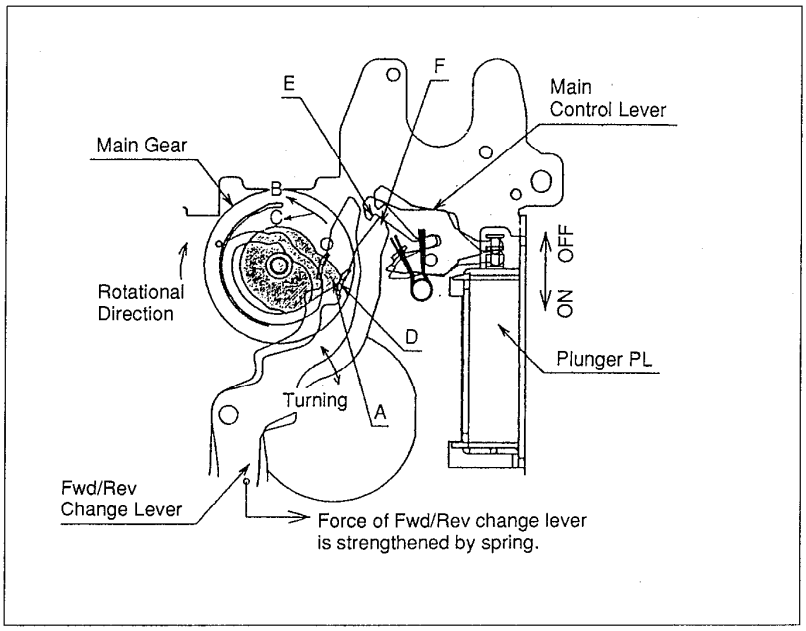


Fig. 7 Fwd/Rev change lever movement

3–2. Fwd/Rev rod movement

3–2–1. Functions of Fwd/Rev rod

The Fwd/Rev rod has the following functions:

1. Pressing the used-side pressure roller against the capstan.
2. Keeping the supply-side reel table gear from getting engaged.
3. Rotating the head.

3–2–1–1. Pressing the used-side pressure roller against the capstan

As shown in Fig. 8, the Fwd/Rev change lever makes Fwd/Rev rod slide to right or left, thereby controlling the pressure roller's position.

In the case of Fwd play, for instance, the Fwd/Rev rod slides to the right and causes the spring gadget A to press the B-part of the Fwd-side pressure roller pressing spring until the Fwd-side pressure roller C is pressed against the capstan.

At this time, the Rev-side pressure roller F is not pressed against the capstan since the Rev-side spring gadget D does not get engaged with the E-part of the Rev-side pressure roller pressing spring.

The same applies to Rev play. But, in this case, all is reverse since the Fwd/Rev rod slides to the left.

3–2–1–2. Keeping the supply-side reel table gear from getting engaged

As shown in Fig. 8, when the takeup gear is engaged with the gear of the reel table, the takeup gear transfers rotation from the flywheel to rotate the reel table.

For Fwd play, the takeup gear H is made to mesh with the gear of the right-side reel table G and the left-side takeup gear I is kept from meshing.

For Fwd play, as shown in Fig. 8, the right-side takeup arm J meshes with the gear of the reel table G by the force of the spring K. On the other hand, the left-side takeup arm L is held at the lower end part M by the Fwd/Rev rod's pawl 0, and the takeup gear I is kept from meshing with the gear of the reel table P.

The same applies to Rev play. But, in this case, all is reverse since the Fwd/Rev rod slides to the left, and the left-side take up gear I meshes with the gear of the reel table P, while the right-side takeup gear H is kept from meshing.

3–2–1–3. Rotating the head

By making the Fwd/Rev rod sliding to right or left, the head pressing spring mounted on the Fwd/Rev rod turns the change gear rotating jointly with the head, thereby causing the head to rotate.

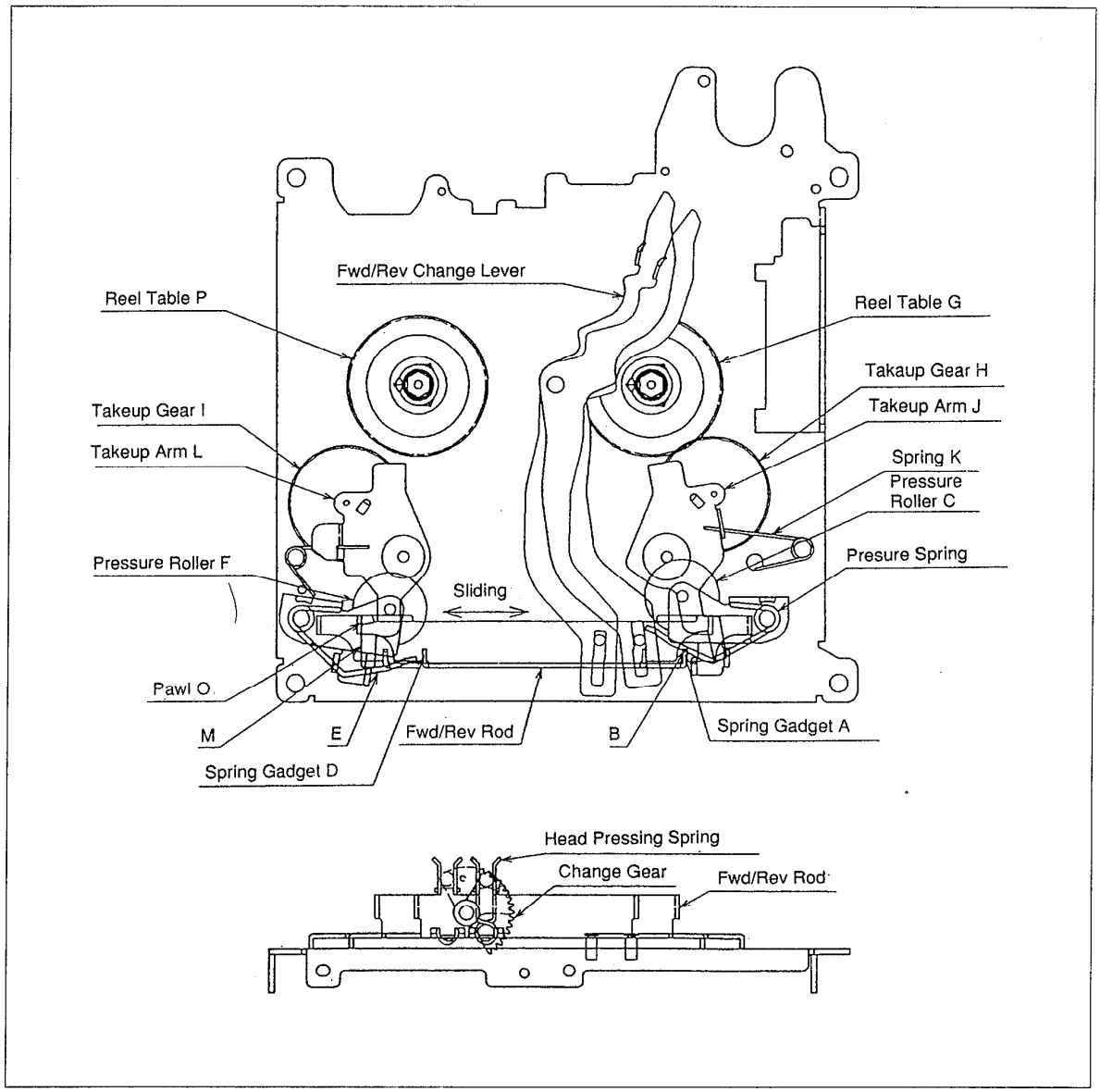


Fig. 8 Fwd/Rev rod movement

3–3. Takeup gear meshing control (Functions of head baseplate)

Besides the above-mentioned Fwd/Rev rod, the head baseplate is also used to control meshing of the takeup gear rotating the takeup reel table for play.

While the Fwd/Rev rod controls meshing of the takeup gear during play, movement of the head baseplate is utilized to control the takeup gear not to get in mesh with the gear of the reel table during STOP, FF (REW), and TPS FF (TPS REW).

As shown in Fig. 9, when the head baseplate is in position other than play, the part A of the head baseplate pushes part B of the takeup arm to keep the takeup gear from getting in mesh with the gear of the reel table.

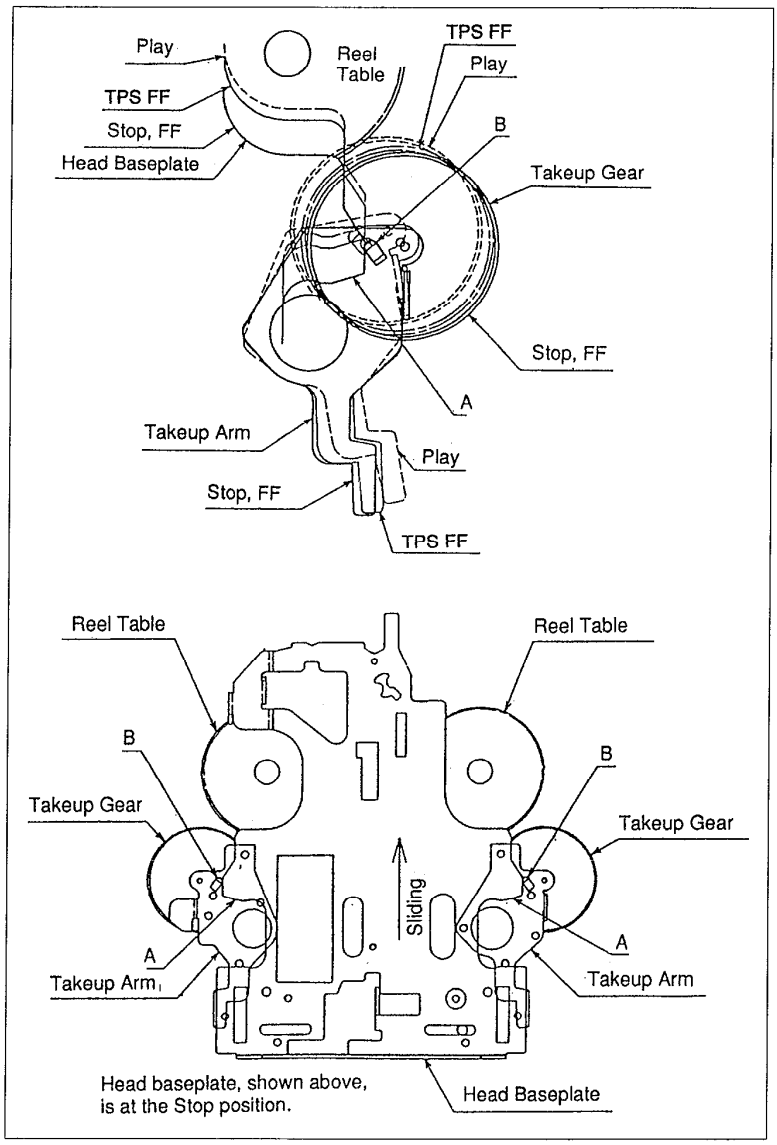


Fig. 9 Takeup gear meshing control

4. Loading/Ejection Mechanism

4–1. Loading and ejection

4–1–1. Loading

(1) When the main gear is at the stop mode station, the gears from the power motor drives LF change gear mesh with the load gear B. This condition allows the cassette loading and ejection by the power motor. (see Fig. 10)

(2) CW rotation of the power motor moves the slider and the ejection pawl to pull in the cassette horizontally.

(3) Further CW rotation causes the cassette holder to descend by the cam mounted on the slider.

- Neutral detection switch SW1 is used to detect the beginning and the end of action. This switch, actuated by the cam provided on the flank of the load gear C and by the EJ detection lever, turns OFF at both ends of loading and ejection..

* Since SW1 turns OFF at the end of loading, it can be used freely at the main gear's stations except the STOP mode station and is also used for the sub-gear's neutral detection.

4–1–2. Ejection

Ejection is carried out by CCW rotation of the power motor. Power Motor stop timing is detected by the neutral detection switch SW1 turning OFF.

4–2. Metal detection switch functions

The metal detection switch has the following functions:

1. Tape loading start detection
2. Normal/Metal tape discrimination

4–2–1. Tape loading start detection

(1) The metal detection switch SW2 is turned ON by the loading detection rod (linked with the eject arm) and the metal detection lever after the tape is ejected.

(2) By slightly inserting the cassette, the eject arm turns and, through the middle of the loading detection rod and metal detection lever, sets SW2 to the OFF position.

(3) When SW2 is turned OFF, the microcomputer detects insertion of the cassette and then the loading action starts.

4–2–2. Normal/Metal tape discrimination

Upon the loading of the cassette, the metal detection switch SW2, which can be turned ON and OFF automatically by the cassette tape.

Since the metal detection lever has a projection to enter the metal detection hole of the cassette, it sets SW2 to ON if the tape is a normal one, and sets SW2 to OFF if the tape is a chrome-dioxide or metal one.

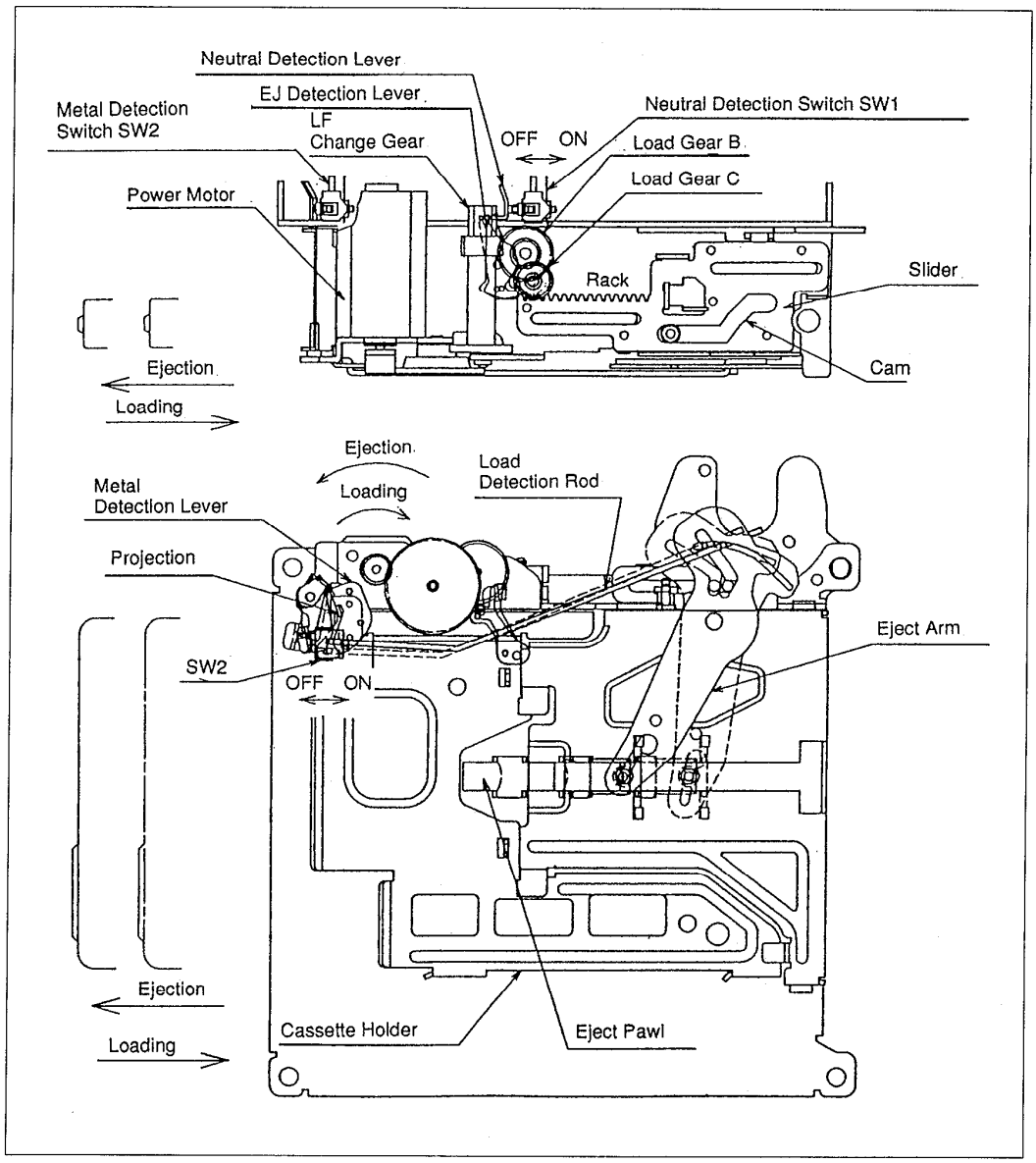
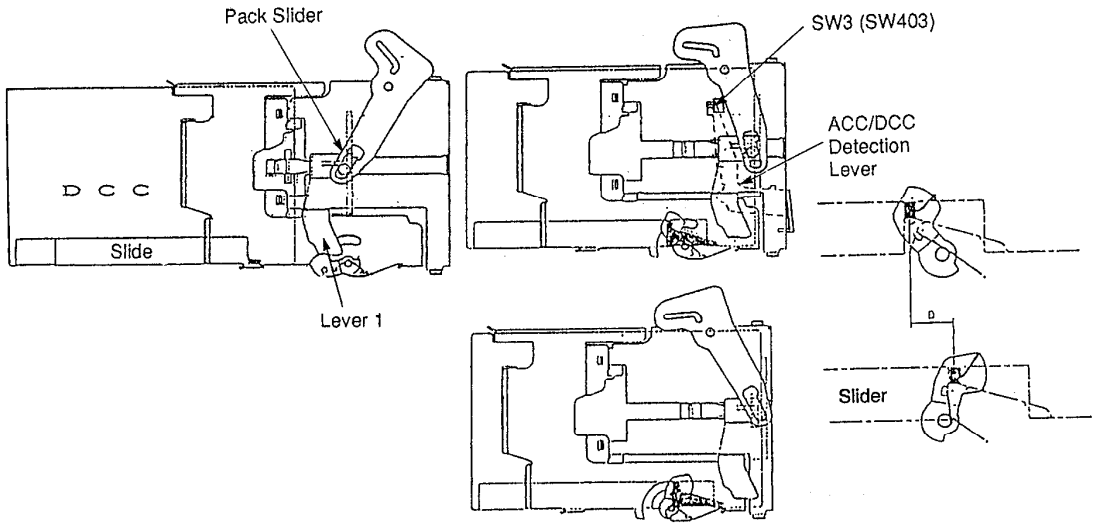


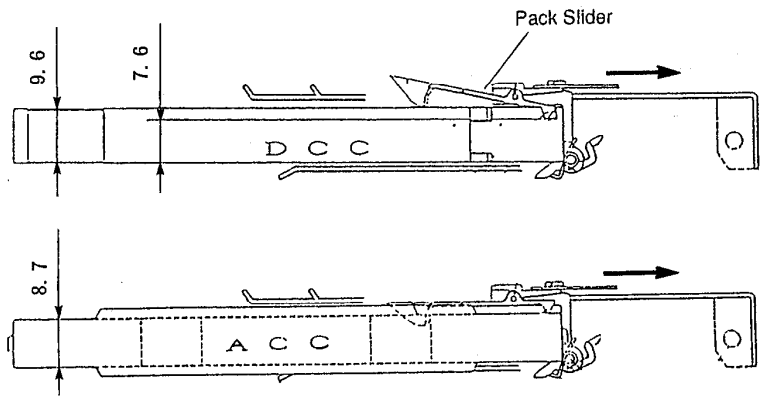
Fig. 10 Loading/ejection mechanism

5. DCC TAPE DETECTION

When the DCC tape is inserted, the pack slider is moved to inward. And the lever (1) is moved for arrow direction shown then the slider of DCC moves for opening tape part.

When the DCC tape is set into the cassette holder, the DCC detection lever moves outward to turn on the DCC/ ACC detection switch SW3 (SW903).

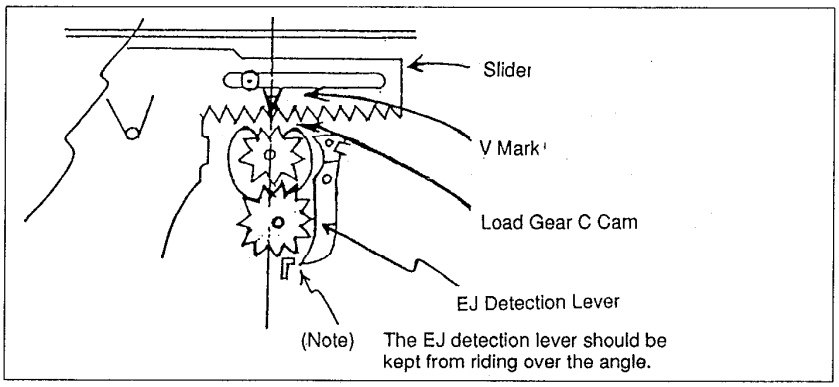




6. Mechanism Mounting & Adjustment Points

6–1. Load gear C mounting instructions

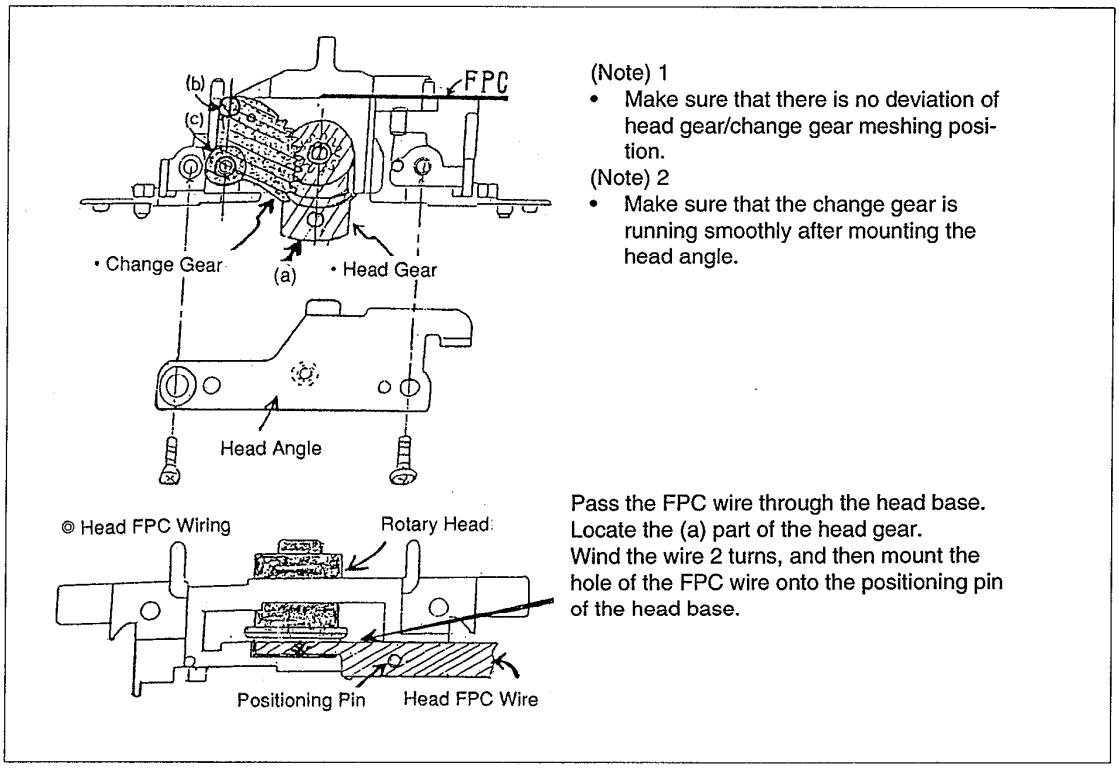
* Align the V mark on the lift slider gear part with the center of the cam part of the load gear C cam.



6–2. Head gear and change gear mounting instructions

(1) Locate the (a) part of the head gear .

(2) Keeping the change gear's (b) and (c) parts in a vertical straight line, make the gear teeth mesh.


(b)
(c)
FPC
• Change Gear
(a)
• Head Gear
Head Angle
© Head FPC Wiring
Rotary Head
Positioning Pin
Head FPC Wire
(Note) 1
• Make sure that there is no deviation of head gear/change gear meshing position.
(Note) 2
• Make sure that the change gear is running smoothly after mounting the head angle.
Pass the FPC wire through the head base.
Locate the (a) part of the head gear.
Wind the wire 2 turns, and then mount the hole of the FPC wire onto the positioning pin of the head base.

4. MECHANISM CONTROL BLOCK

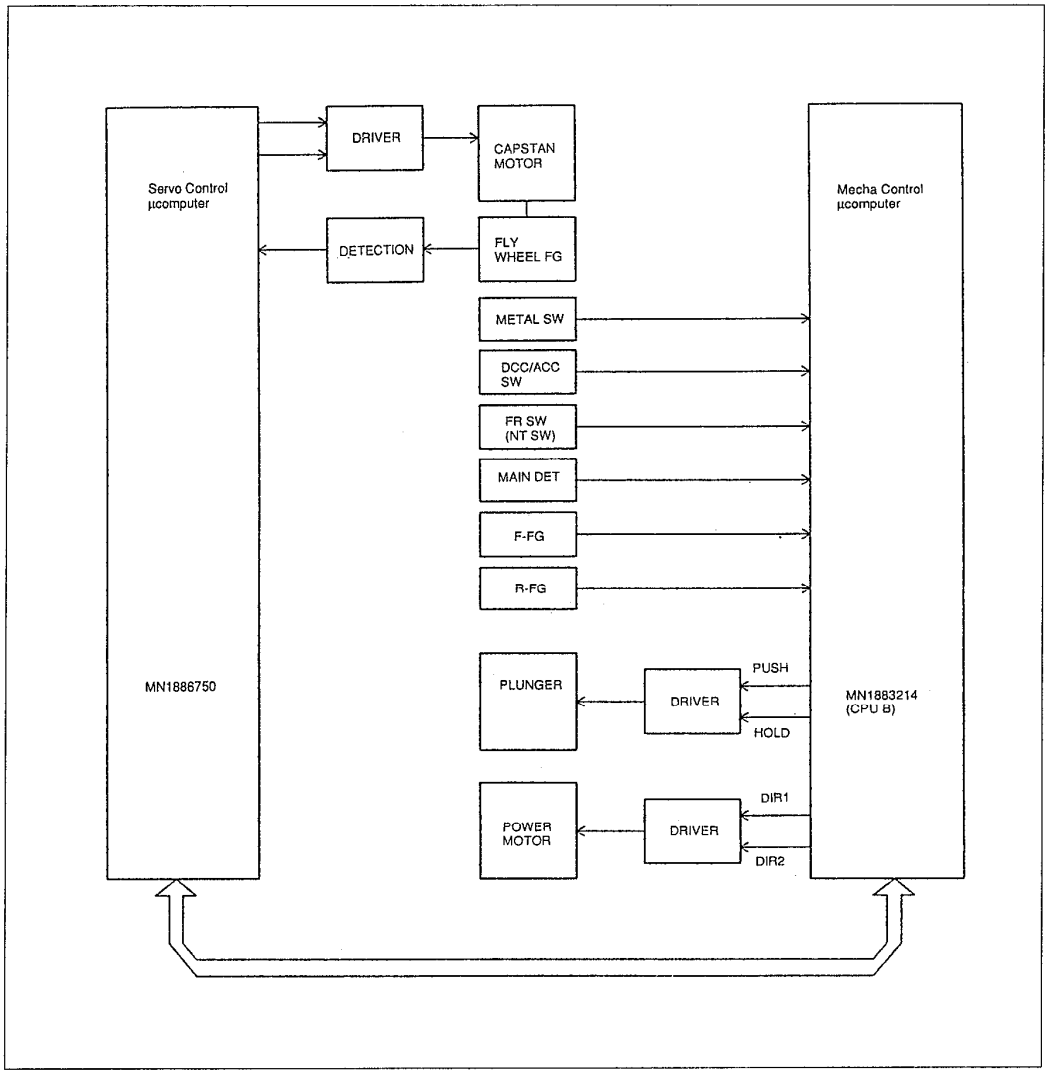


Fig. 10 Mechanism control block

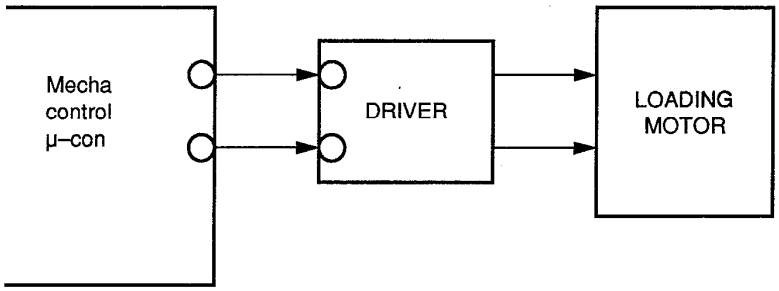
1. CAPSTAN MOTOR CONTROL

Servo μ-con is controled by pin 35 and 36 of main microcomputer and servo μ-con controls capstan motor.

MAIN μ-CON OUTPUT		MAIN μ-CON INPUT		MOTOR CONDITION
(Pin 36) Pspd_set1	(Pin 35) Pspd_set2	(Pin 55) Pspd_mon1	(Pin 54) Pspd_mon2	
L	L	L	L	NORMAL SPEED
H	L	H	L	0.5 TIMES SPEED
L	H	L	H	2 TIMES SPEED
H	H	H	H	STOP

2. Loading Motor Control

Forward and reverse of the power motor is controled by pin 66 and pin 67 of the mechanism μ-con.



Control Losic

μ-CON OUTPUT		DRIVER OUTPUT		MOTOR CONDITION
Pin 66 (Pdir1)	Pin 67 (Pdir2)	POWER M+	POWER M-	
L	L	"OFF" state	"OFF" state	STOP
H	L	H	L	FORWARD
L	H	L	H	REVERSE
H	H	L	L	BRAKE

Plunger (solenoid) Control

Solenoid is controled by pin 64 and pin 62 of Mecha–μ-con.

Pin 64 ("H") ..... Solenoid Active Mode

Pin 62 ("H") ..... Solenoid Hold Mode

Plunger control is as shown below.

Plunger ON → Pin 64 : H

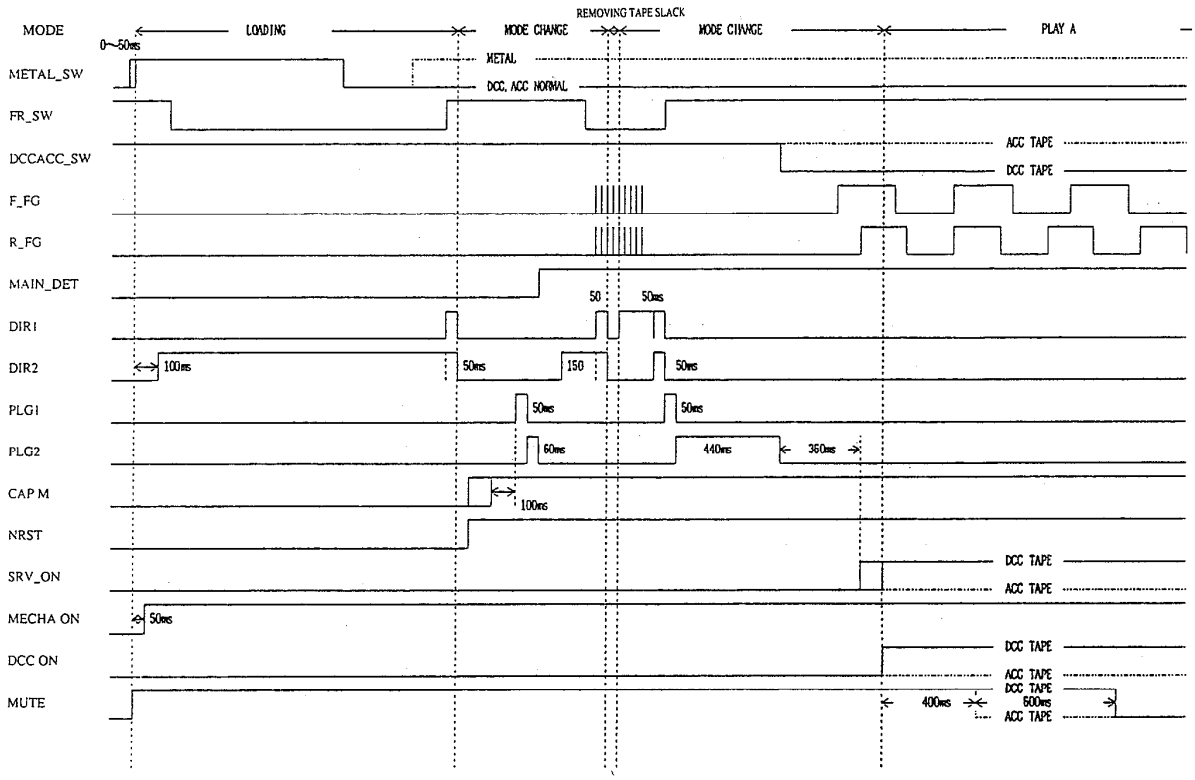
50 ms later → Pin 64 : L

Pin 62 : H

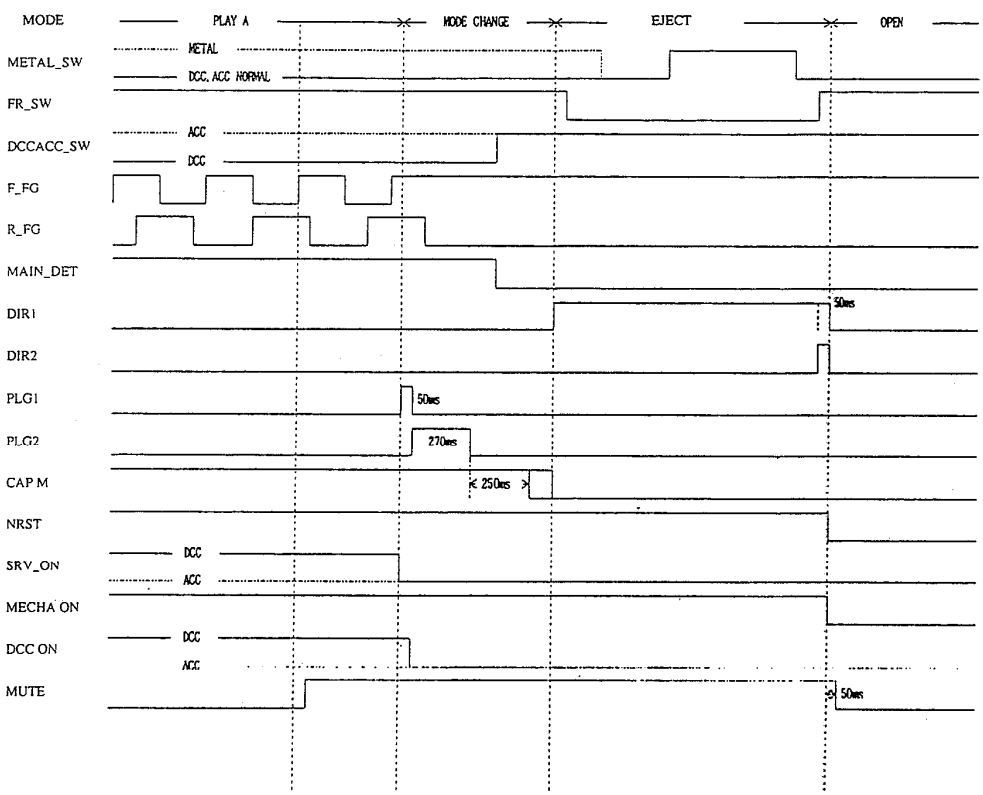
Plunger OFF → Pin 62 L

5 DECK TIMING CHART

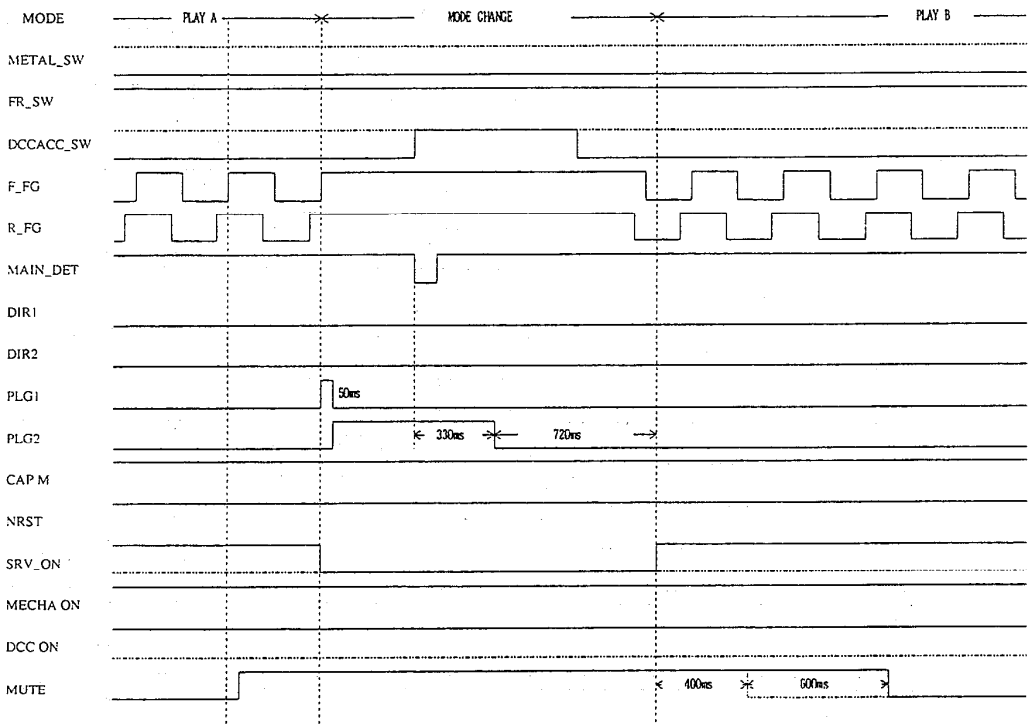
1. Loading → Removing tape slack → PLAY A



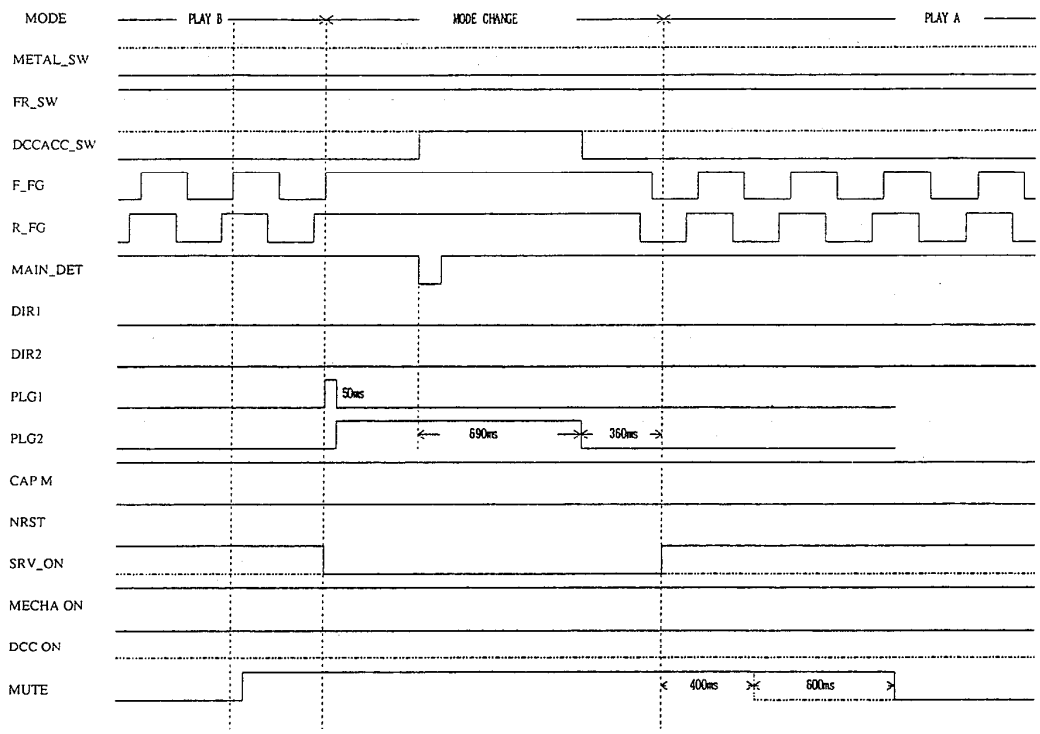
2. PLAY A → EJECT



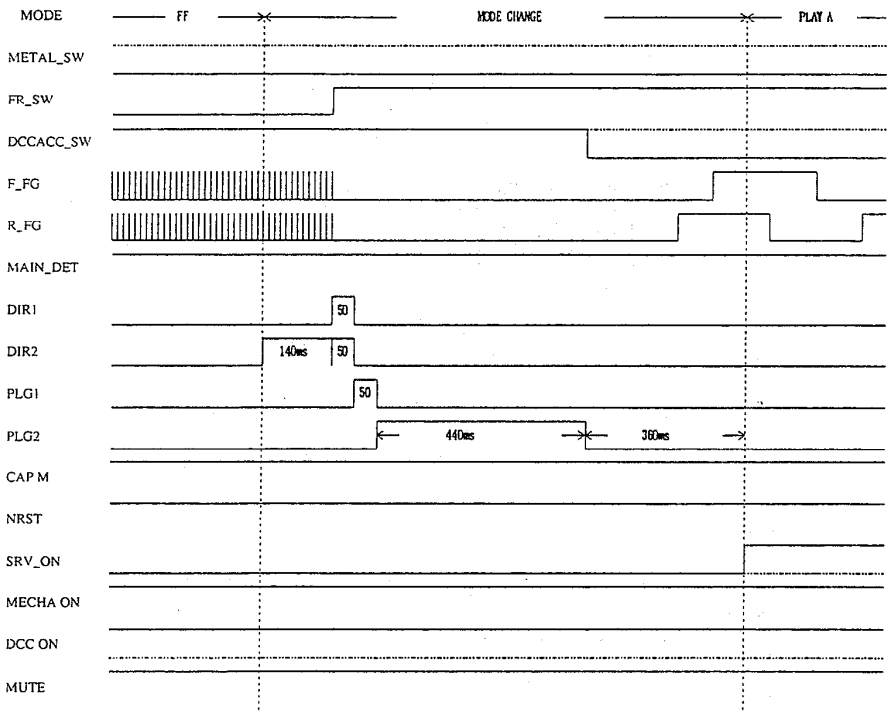
3. PROGRAM CHANGE (A → B)



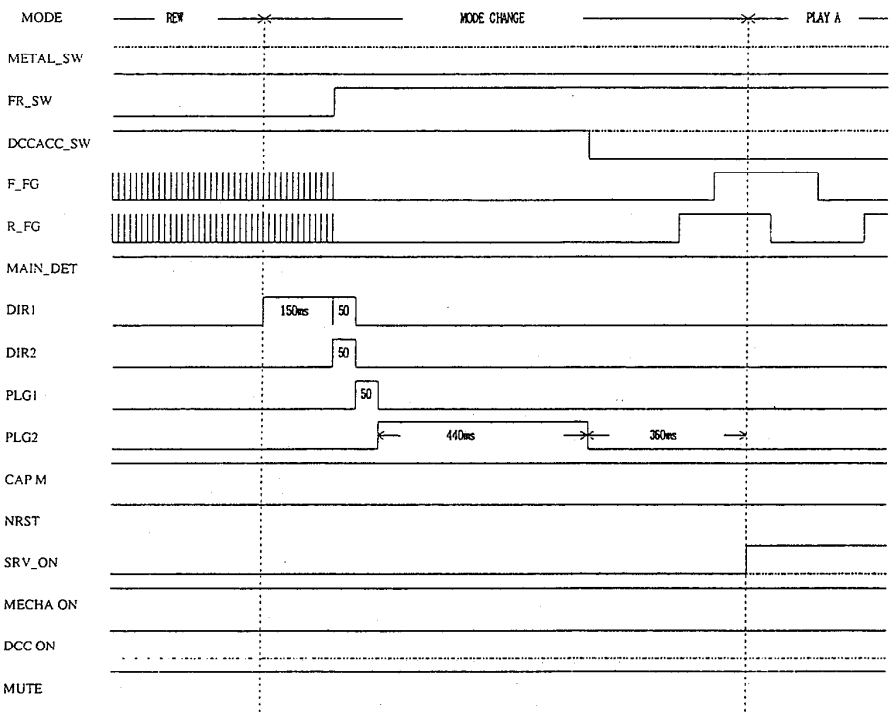
4. PROGRAM CHANGE (B → A)



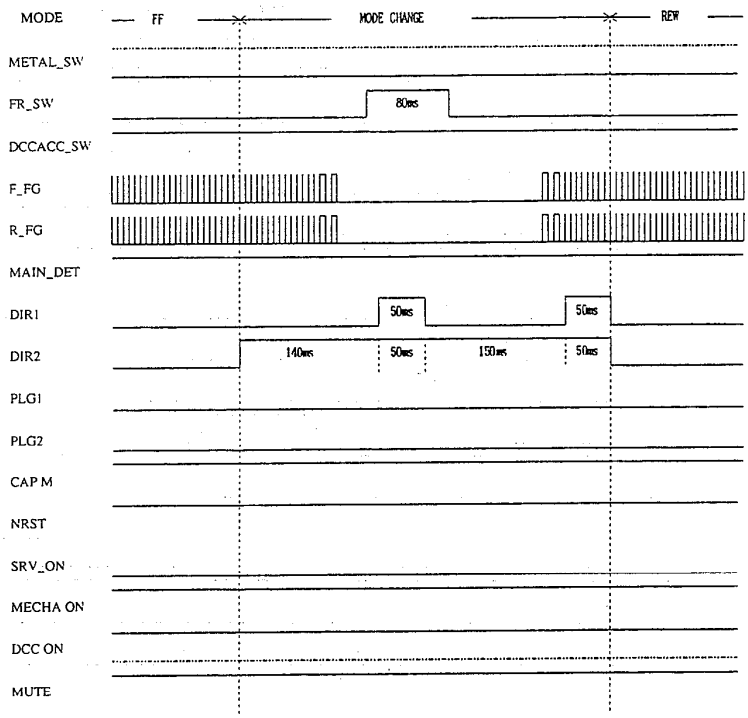
5. FF → PLAY A



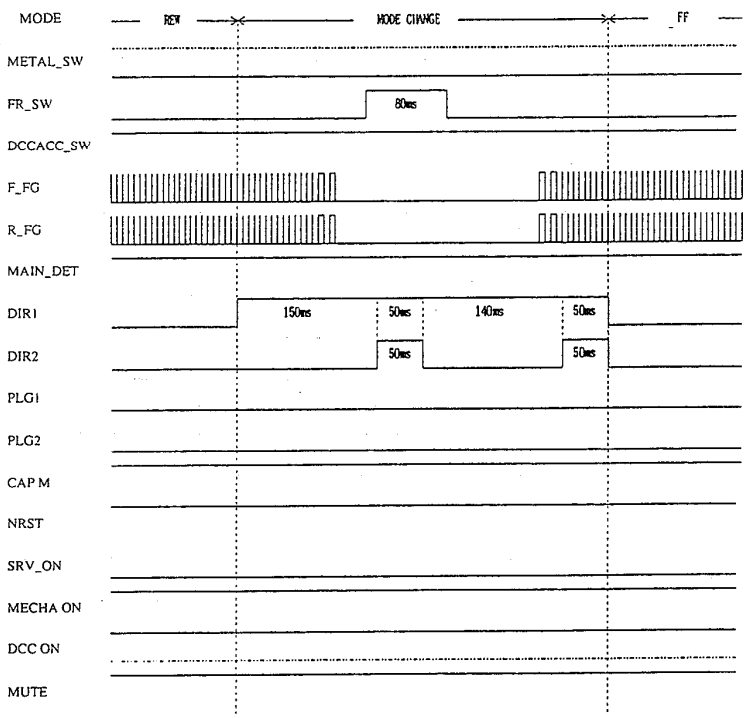
6. REW → PLAY A



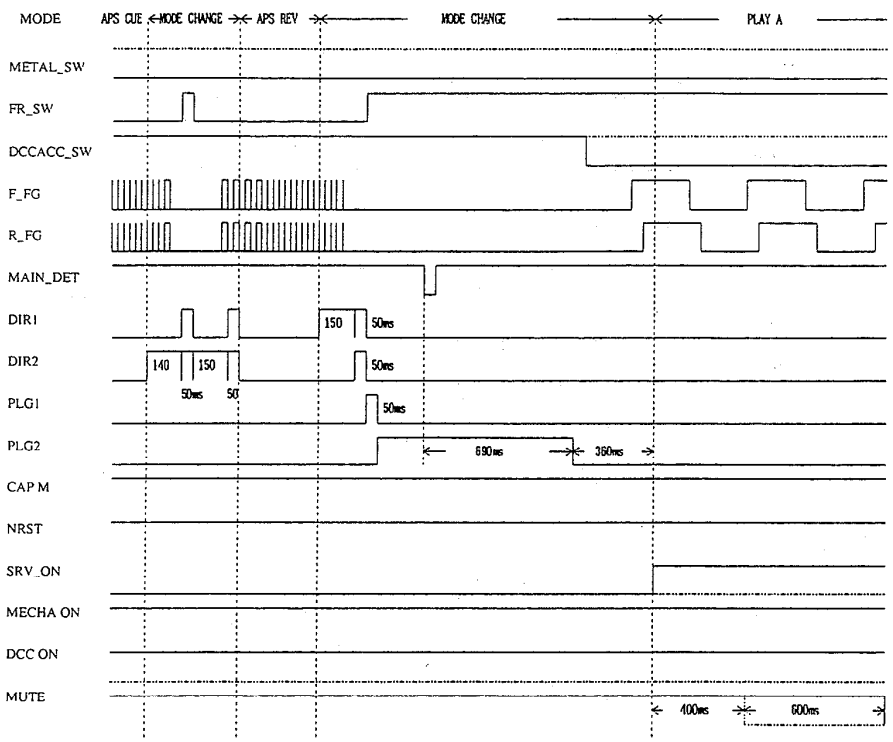
7. FF → REW



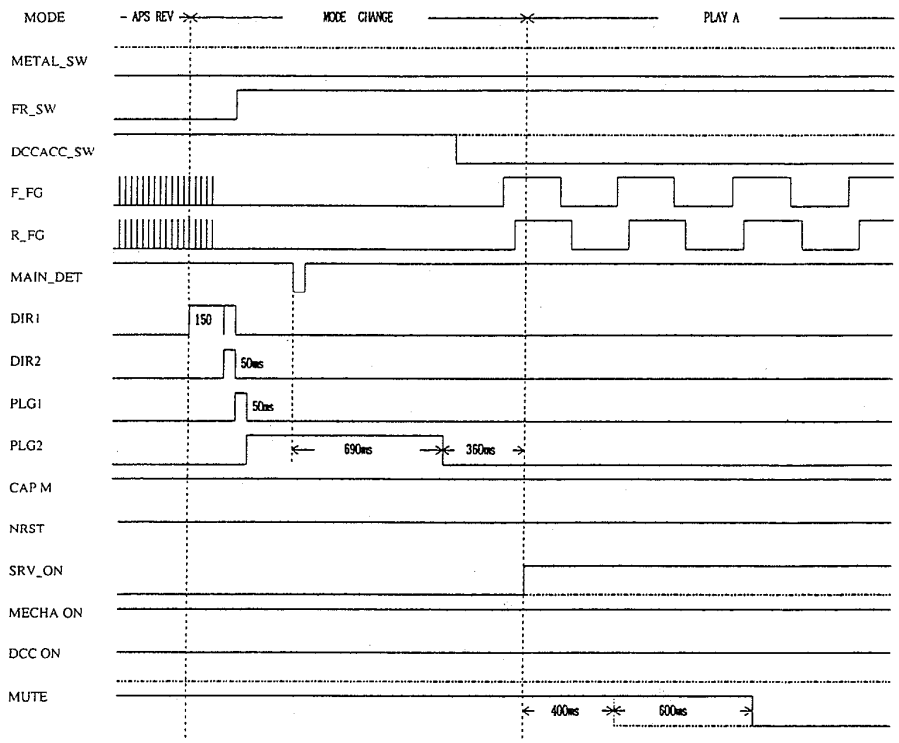
8. REW → FF



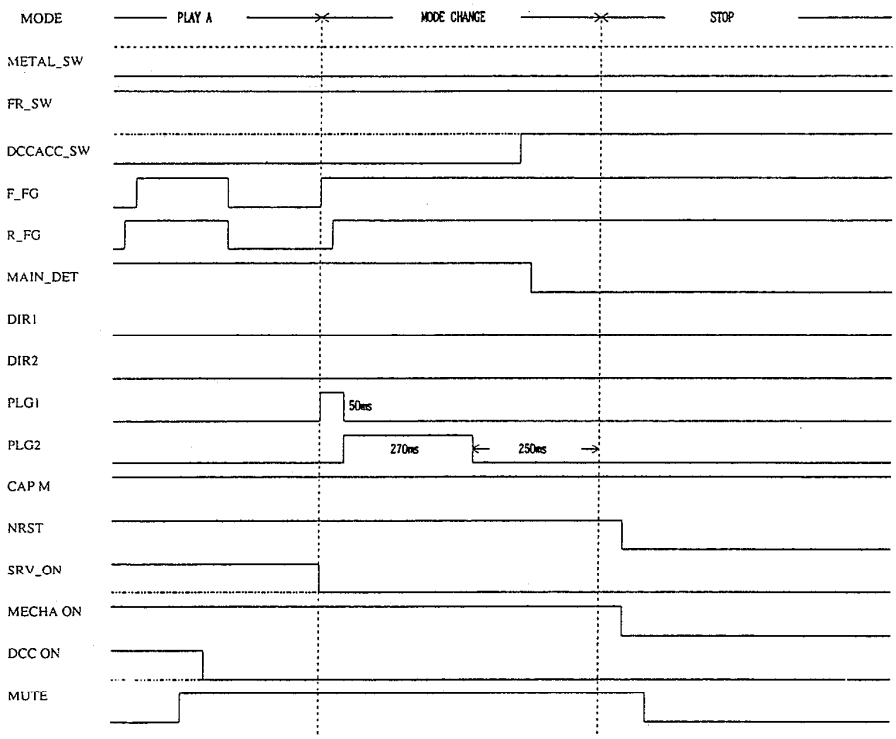
9. APS_CUE → APS_REV → PLAY_A



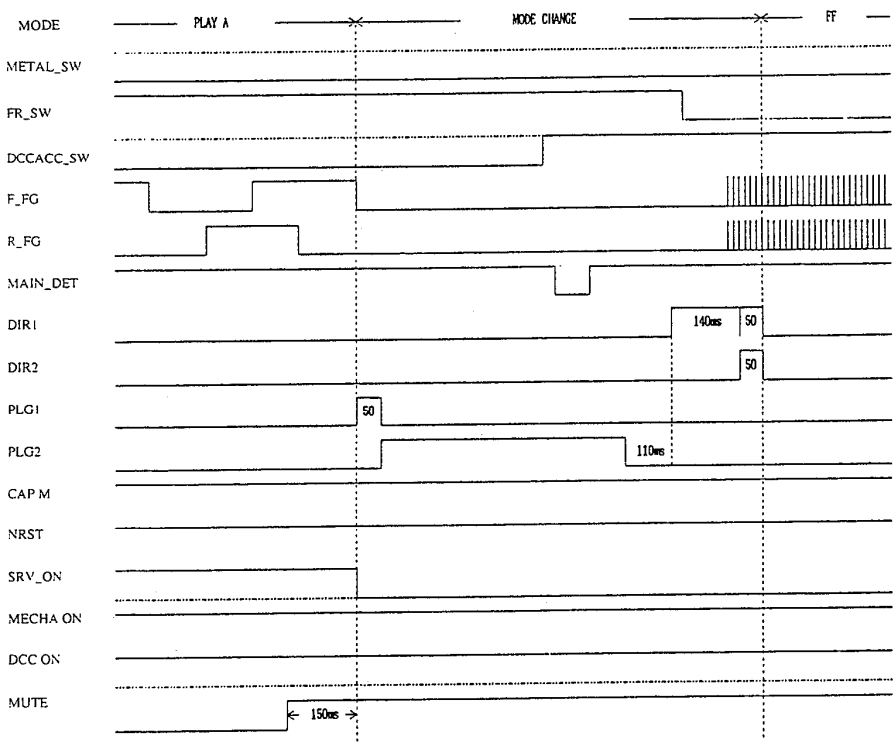
10. APS_REV → PLAY_A



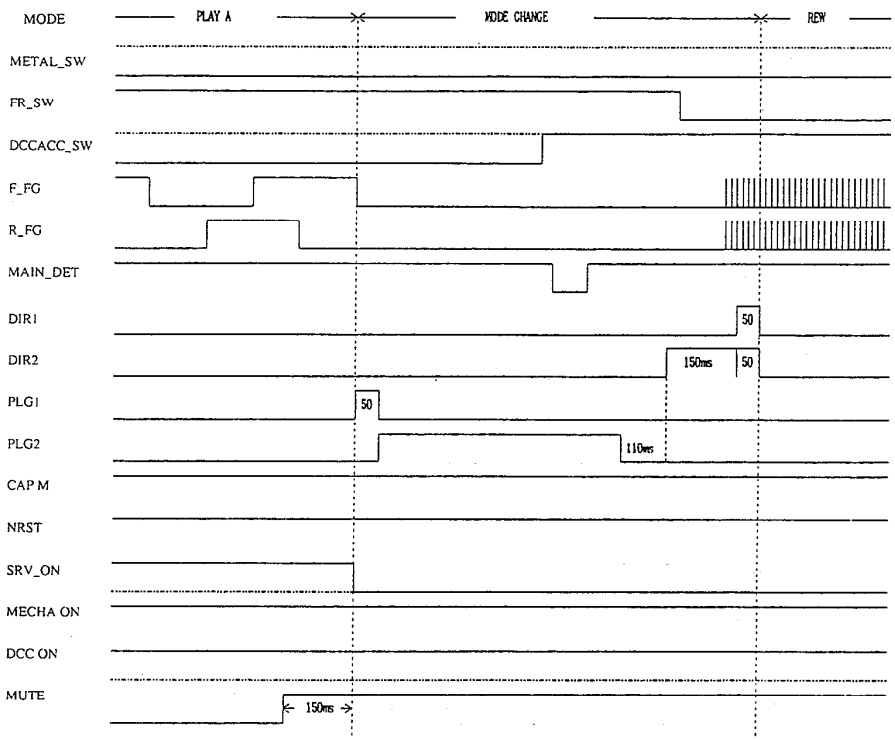
11. PLAY_A → STOP



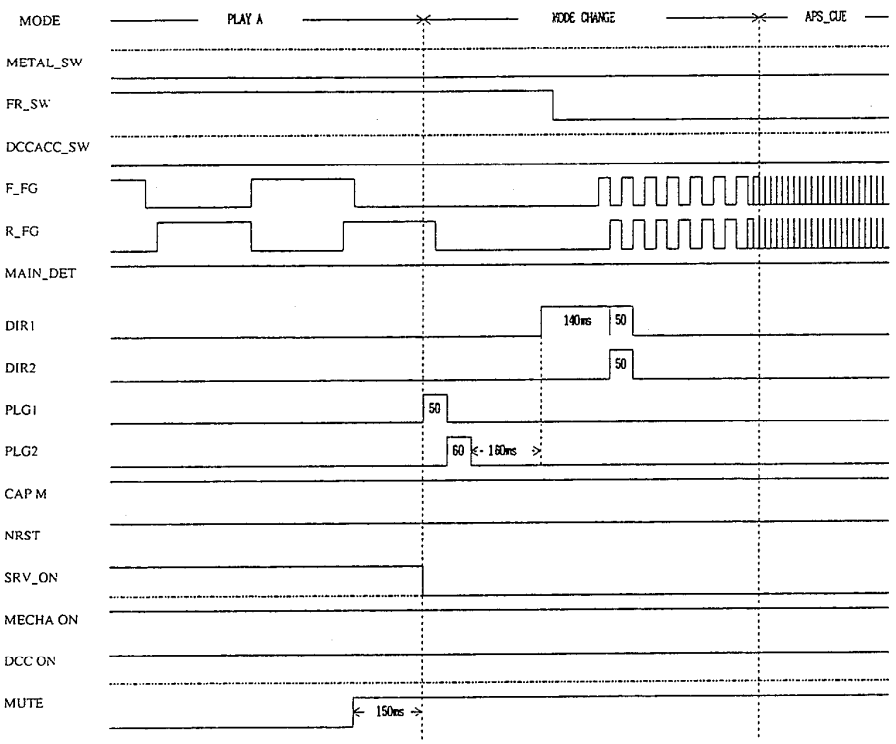
12. PLAY A → FF



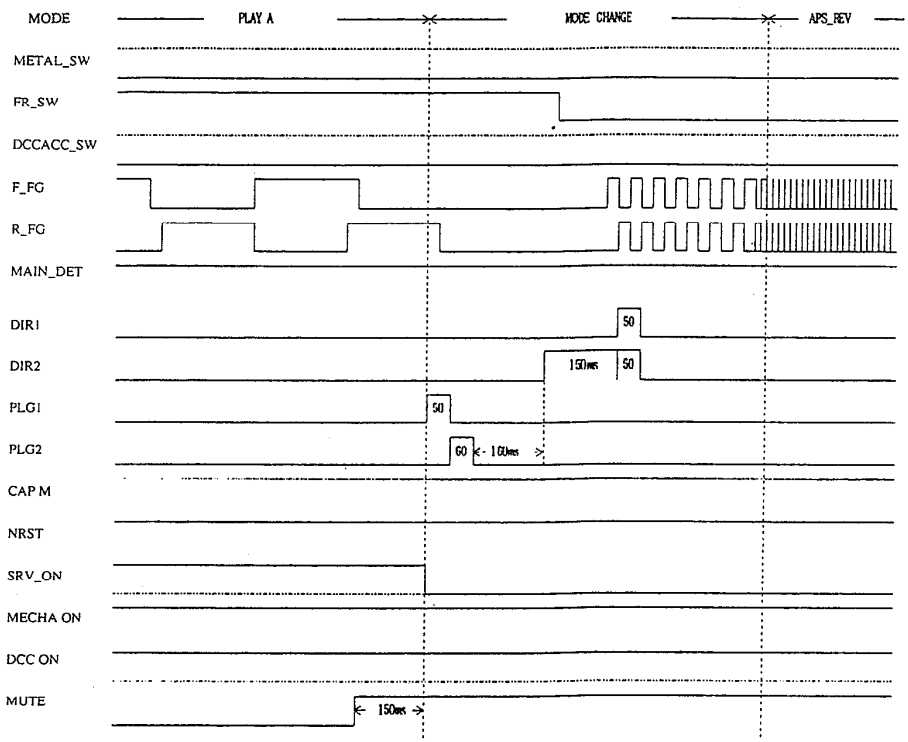
13. PLAY A → REW



14. PLAY A → APS CUE



15. PLAY A → APS REV



EXPLANATION OF DCC CIRCUIT

1. Flow of Signals and Function of Each Block

DDC Data Signal Line

- Data taken out from the head is input to IC201 Pins ⑪, ~ ⑳ IC201 is a read amplifier sending data through BPF (which allows effective bands only) built in this IC. Then the data is output from Pin ③ (RDMUX).
- Data input to DEQ IC13 Pin ⑤ (PBDAT) undergoes waveform equalization (waveform shaping) in IC13, and respective CH data are individually output from Pins ㉒ ~ ㉚
- CH data input respectively to (DDSP) IC7 Pin ㉒ ~ ㉚ are demodulated (10 → 8), and when each CH data is stored in DRAM (IC1) temporarily and read out, the cross interrib is released and the data is output through IC9 Pin ⑯ (SBDAT).
- DATA input to SBC IC12 Pin ㊸ is reformed into the PASC data format in IC12, and after the bit-compressed data is extended to the original state, it is output from Pin ㉟ (FDATC).
- Data input to (ADAS) IC8 Pin ㉝ to calculates the masking power of the sub-band signals and adds the masking threshold, and the data is output from Pin ㉞ (FDATF).
- Data input to SBF IC10 & IC11 to split a single broad-hand digital audio signal into 32 sub-bands or combining 32 sub-band into a single broud-band digital audio signal and the data output from Pin ㉚ (SDAT).
- Data input to the digital filter (DF) IC605 Pin ㉒ undergoes digital filtration and LCH/RCH separation in IC605, the LCH data is output from Pin ⑭, and the RCH data from Pin ⑬. These are input to D/A converter (IC606) Pins ② and ③, returned into analog signals, output from Pin ⑥ (LCH) and Pin ⑧ (RCH), and after passing through LPF, they are supplied to L/RCH LINE OUT terminals.

ACC Signal Line

- The analog signals taken out from the head, is input to playback amp IC202 Pins ③ and ⑤. The LCH and RCH signals are output from Pins ① and ⑦ respectively, and passing through the Dolby IC (IC203), they are supplied to LCH/RCH LINE OUT terminals.

Outline of Signal Line (DCC/ACC)

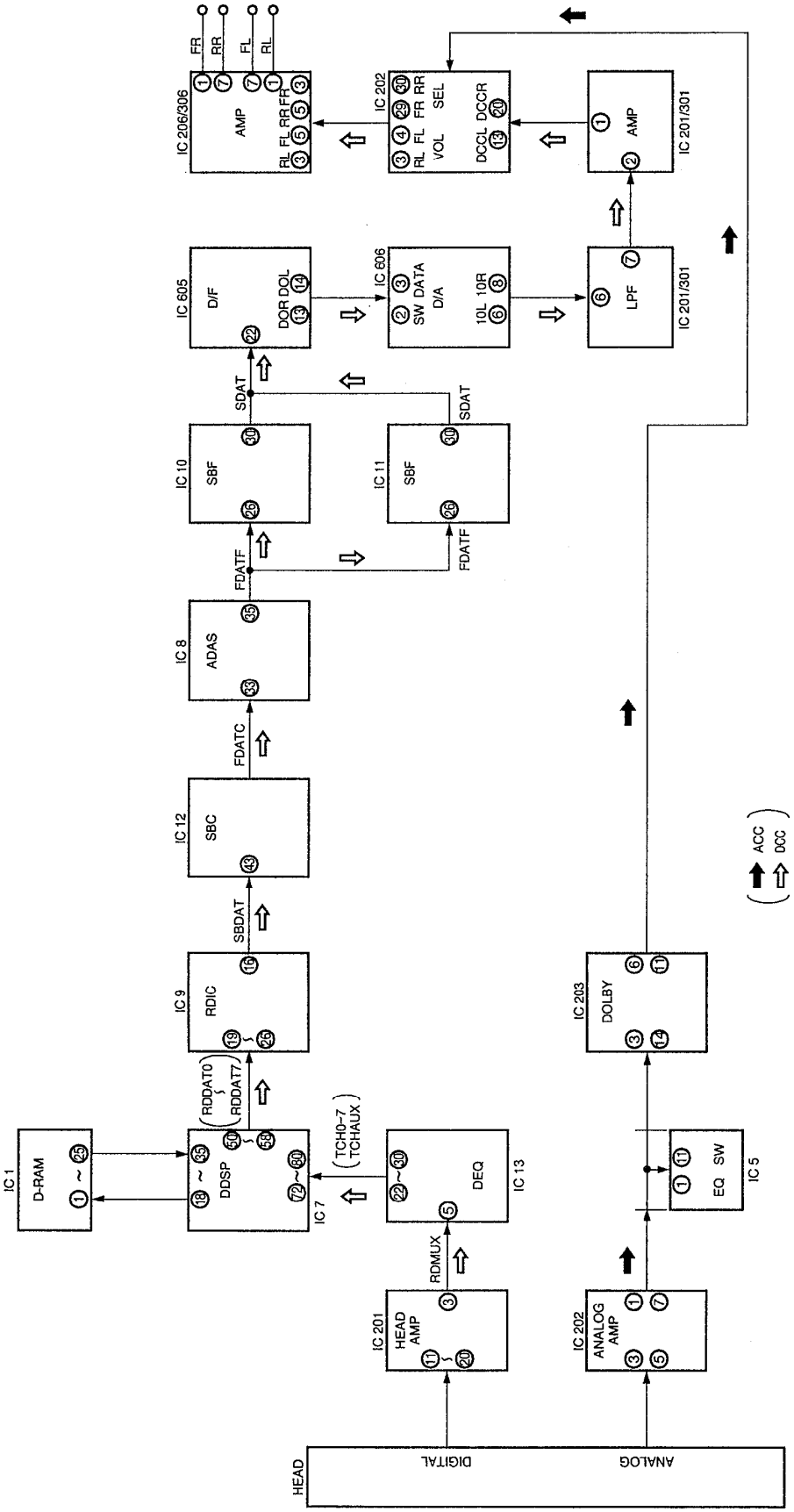


Fig. 1

2. BLOCK DIAGRAM OF DCC

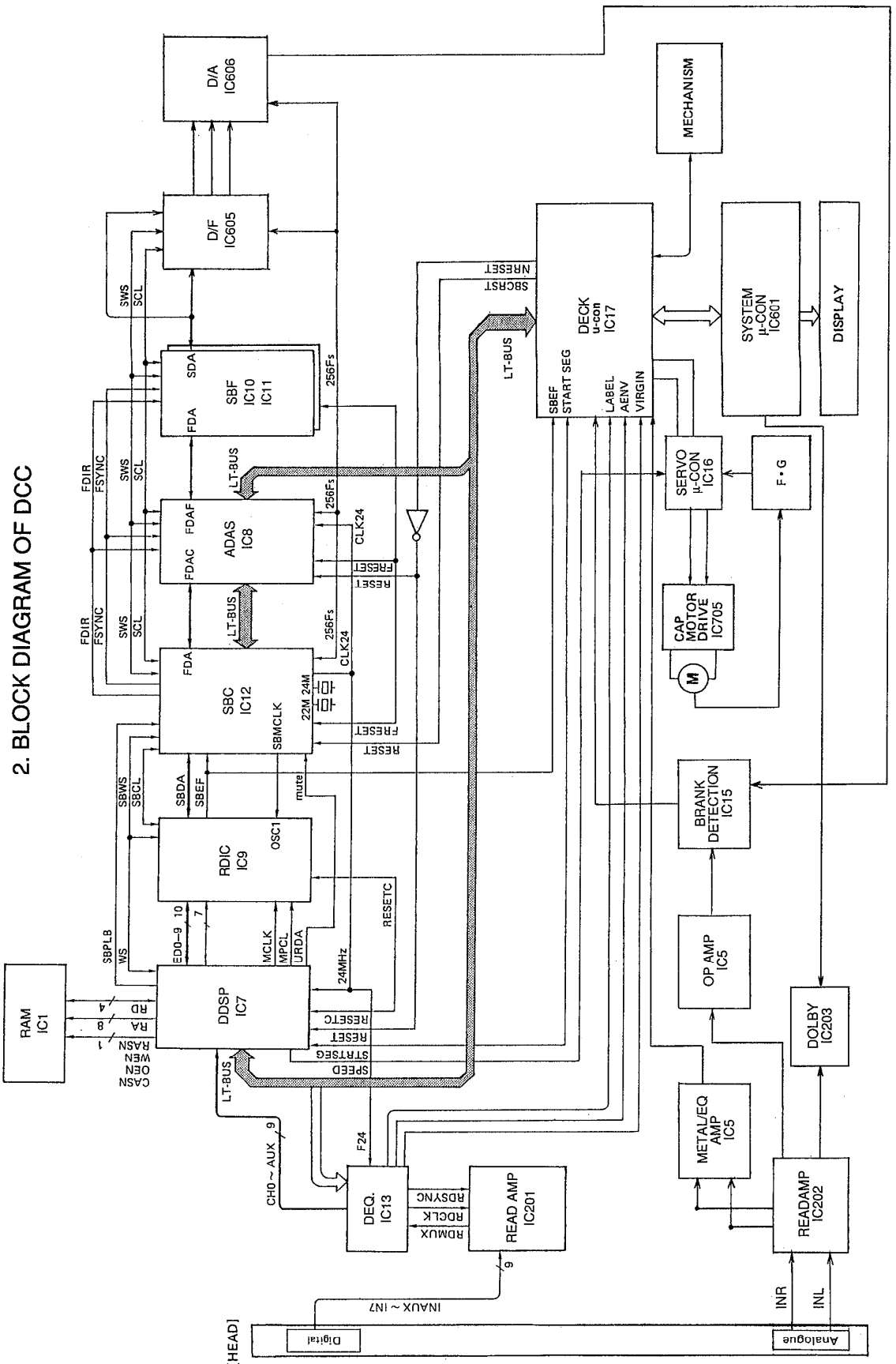


Fig. 2

3. Descrption of Signal Names

SIGNAL NAME	FUNCTION	SIGNAL FLOW	Freq.	EXPLANATION
FDA FDAC	FILTERED DATA FILTERED DATA	SBF → ADAS ADAS → SBC		DATA TRANSFER IN I²S FORMAT, CARRING 32 SUB-BAND CHANNELS DIGITAL AUDIO DATA.
SWS	WORD SELECT	SBC → ADAS SBF ADC D/F	fs	SBC IS MASTER IN PLAY MODE.
SCL	SERIAL CLOCK	SBC → ADAS SBF ADC D/F	64 fs	BIT CLOCK FOR I²S INTERFACE
FSYNC	FILTER SYNC.	SBC → SBF SBC → ADAS	fs/32	SBC PERMIT ONLY TRANSFER OF SUB-BAND 0 DATA DURING FSYNC.
S24 (CLK24)	MASTER CLOCK	SBC → DDSP DEQ	24.576 MHz	F24 IS TO DETERMINE THE LENGTH OF TYPE FRAME AND INTER FRAME GAP.
256 fs	SYSTEM CLOCK	SBC → SBF ADAS ADC DAC	256 fs	IN PLAY MODE, SBC IS THE MASTER AND SUPPLIES 256 fs.
FDIR	DIRECTION CONTROL	SBC → SBF ADAS	H/L	FDIR = 1 (DECODE MODE/PLAY) FDIR = 0 (ENCORE MODE/REC)
SBCL (CLAB)	SUB-BAND CLOCK	SBC → ERC0	64 fs	SBCL IS PART OF I²S INTERFACE AND PROVIDES THE BIT CLOCK.
LT-BUS	LTDATA	µC → ADAS DEQ DDSP		SERIAL DATA LINE
	LTCONT0 LTCONT1			CONTROL LINE OF LT INTERFACE FROM MICROCONTROLLER.
	LT CLOCK			BIT CLOCK FOR THE LT INTERFACE.
ED0 ~ ED9	ERCO DATA LINE	DDSP → ERCO		PARALLEL DATA FOR SYMBOL TRANSFER (SAME AS DATA 0 ~ 7/FLAG 1 ~ 2)
SBEF	SUB-BAND ERROR FLAG	ERC0 → SBC		ERROR FLAG TRANSFERRED TO SBC
REST	RESET			HARDWARE RESET
LT SUBBUS	LT INTERFACE	ADAS → SBC		LT-INTERFACE FOR COMMUNICATION. ADAS IS THE MASTER
MCLK	MASTER CLOCK	DDSP → ERC0	6.144 MHz	THIS CLOCK (128 fs) IS USED FOR THE SYMBOLS TRANSFER.
MPCL	CLOCK PHASE REFERENCE	DDSP → ERC0	3.072 MHz	THIS CLOCK (64 fs) IS USED FOR CLOCK PHASE REFERENCE SIGNAL.
RDMUX	READ MUCTIPLEX	READA → DEQ		READ MULTIPLEXER OUTPUT.

Descrption of Signal Names

SIGNAL NAME	FUNCTION	SIGNAL FLOW	Freq.	EXPLANATION
RDCLK	READ CLOCK	DEQ → READ AMP	960 MHz	DATA CLOCK FOR READ AMP. DATA OF 8 CH AND 1 AUX CH IS TRANSFERED DURING 10 RDCLK PERIODS
RDSYNC	READ SYNC.	DEQ → READ AMP		CONTROL OUTPUT OF DEQ TO SYNCHRONIZE THE READ AMP.
CH0 ~ CH7	DATA LINE	DEQ → DDSP		REQ CHANNEL n OUTPUT
SPEED	SPEED CONTROL	DDSP → SERVO		PWM CONTROL SIGNAL FOR CAPSTAN
STRTSEG	START SEGMENT	DDSP → μc		STRTSEG IS USED AS A TIMING FOR TRANSFER OF SYSINFO AND AUX
SBDIR	SUB BAND DIRECTION	DDSP → SBC		DIRECTION OF DATA FLOW BETWEEN ERCO AND SBC ON SBDA LINE
LABEL	LABEL	DEQ → μc		SEARCH MODE LABEL DETECTION LABEL FOUND IN THE AUX-CH
AEMV	ALTERNATING ENVELOPE	DEQ → μc		MONITORS DURING SEARCH MODE THE START OF A TRACK (FROM AUX-CH)
VIRGIN	VIRGIN DETECTION	DEQ → μc		INFORM THE μc A BLANK TAPE IS INSERTED
RDATA 0 ~ 3 (RD)	RAM DATA BUS	DDSP → DRAM		BATA BUS LINE.
ADRS0 ~ 7 (RA)	ADDRESS LINES	DDSP → DRAM		8 ADDRESS LINES TO DRAM TO LOCATE ADDRESS FOR WRITING DATA INTO OR READING DATA FROM MEMORY
AUX	AUX-CH OUTPUT	DEQ → DDSP		SLICED OUTPUT FROM DEQ OF AUX-CH DATA
DOL/DOR	DIGITAL OUTPUT	D/F → D/A		SERIAL DATA OUTPUT
BCK0	BIT CLOCK	D/F → D/A		CLOCK SIGNAL
WCK0	WORD CLOCK	D/F → D/A	3.072 MHz	INDICATE WHETHER DATA FOR L-CH, OR R-CH
SBMCLK	SUB-BAND MASTER CLOCK	SBC → ERCO	6.144 MHz	

4. Operation of Digital Block

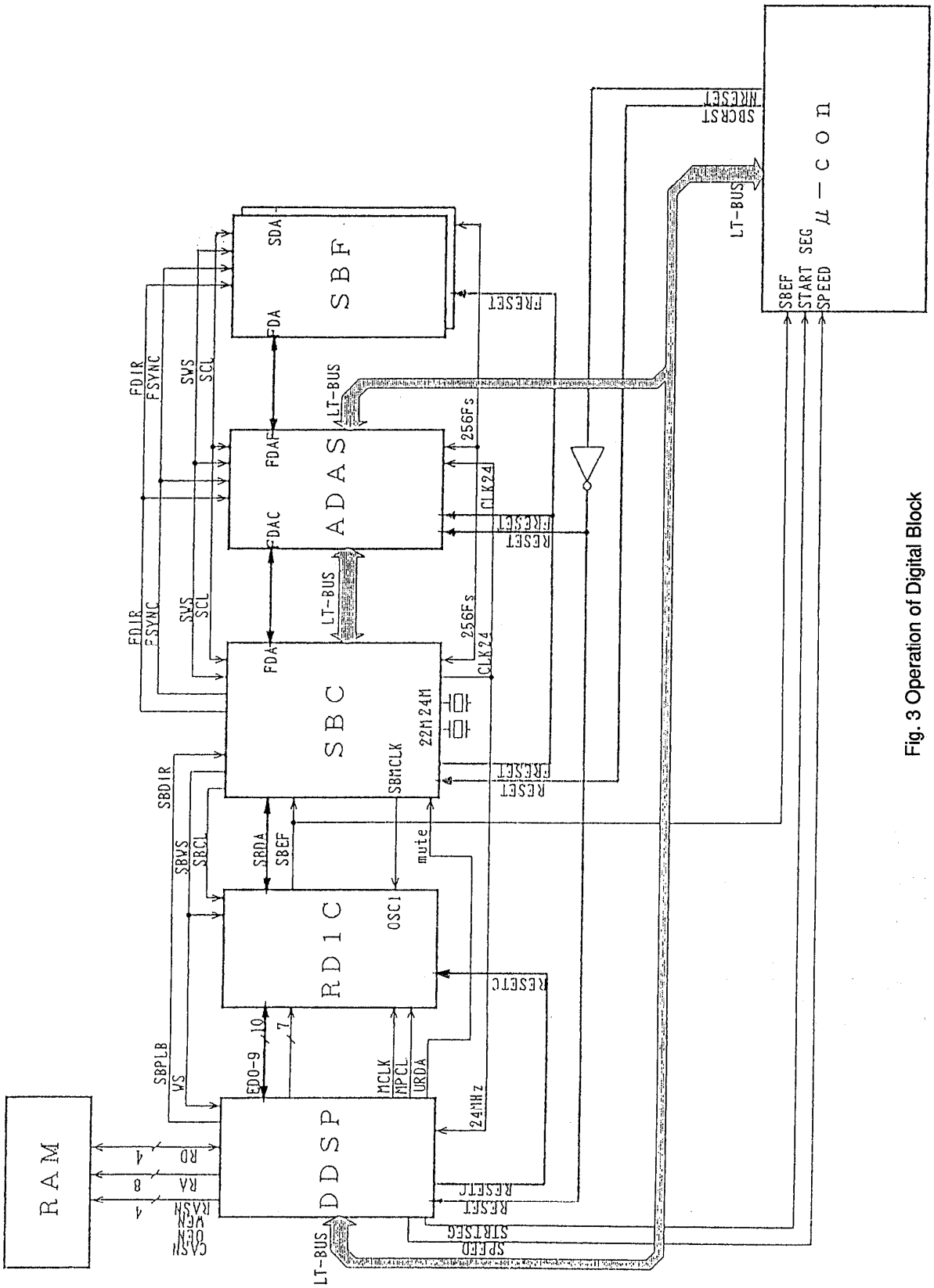


Fig. 3 Operation of Digital Block

PASC/Precision Adaptive Sub-band Coding

Precision Adaptive Sub-band Coding achieves highly efficient digital encoding of audio signals by using an algorithm based on the characteristics of the human auditory system.

The broad-band audio shignal is split into 32 sub-band signals during encoding. For each of the sub-band signals the masking threshold is calculated. The samples of the sub-bands are incorporated in the PASC signal with an accuracy that is determind by the singal to masking threshold ratio for that sub-band.

DDSP/Digital Drive Signal Processing

Performing digital signal processing within the DCC (Digital Compact Cassette) system, the DDSP (Digital Drive Signal Processing; SAA2041) device possesses control, address generation and data formation functions within the system. Its main functions include control of the ERCO (SAA2031) device together with the processing of data from the DEQ (SAA2051).

SBC/Sub-band Coder and Decoder

When encoding audio data, the SBF (sub-band filter, SAA2001) devices split the incoming signals at the sample frequency (f2) into 32 sub-bands. The SBC (Sub-band Coder and Decoder, SAA2021) performs the signal encoding. Different bit-rates can be used for data transfer.

During the decoding of data, the SBC (SAA2021) reconstructs the sub-band signals for application to the SBF (SAA2001) devices which reconstitute the sub-band signals into a single digital audio signal.

The input and output system data are digital samples of an audio signal represented in 24-bit two's complement. The sub-band samples are represented in 24-bit two's complement notation.

ERCORR/Error Correction

The Error Correction/Decoder is designed for Reed Solomon codes over GF (256) of distance 5 or 7 at a maximum code word length of 32 symbols:

ADAS/Adaptive Allocation and Scaling

The PASC system calculates the masking power of the sub-band signals and adds the masking threshold. Sub-band signals with power below this threshold denote information to be discarded. Non-masked signals are coded using floating point notation in which a mantissa corresponds in length to the difference between peak power and masking threshold. The process is repeated for every PASC frame and is known as the Adaptive Allocation of the available capacity.

SBF/Sub Band Filter

Per forming the splitting or combining function in the Precision Adaptive Sub-band Coding (PASC) system, the SAA2001 is a Sub-Band Filter (SBF) intended for use in conjunction with the ADAS (Adaptive Allocation and Scaling; SAA2011) and SBC (Sub-band Coder/ Decoder; SAA2021) devices. It is capable of splitting a single aroar-band digital.

In a complete stereo (or 2-channel mono) PASC system, two SAA2001 devices are required; one for each channel.

5. DCC Read Amplifier

Feedback Amplifiers

Two feedback amplifiers are provided for driving a coil in the Compact Cassette MRH. This provides a feedback loop in order to improve the linearity of the analog audio response.

Multiplexer

The IC employs a multiplexer circuit to switch the digital channels, sequentially, to the output. The effective sampling frequency is one tenth of the clock frequency at RD CLK (pin 6). A timing diagram is given in Fig. 5

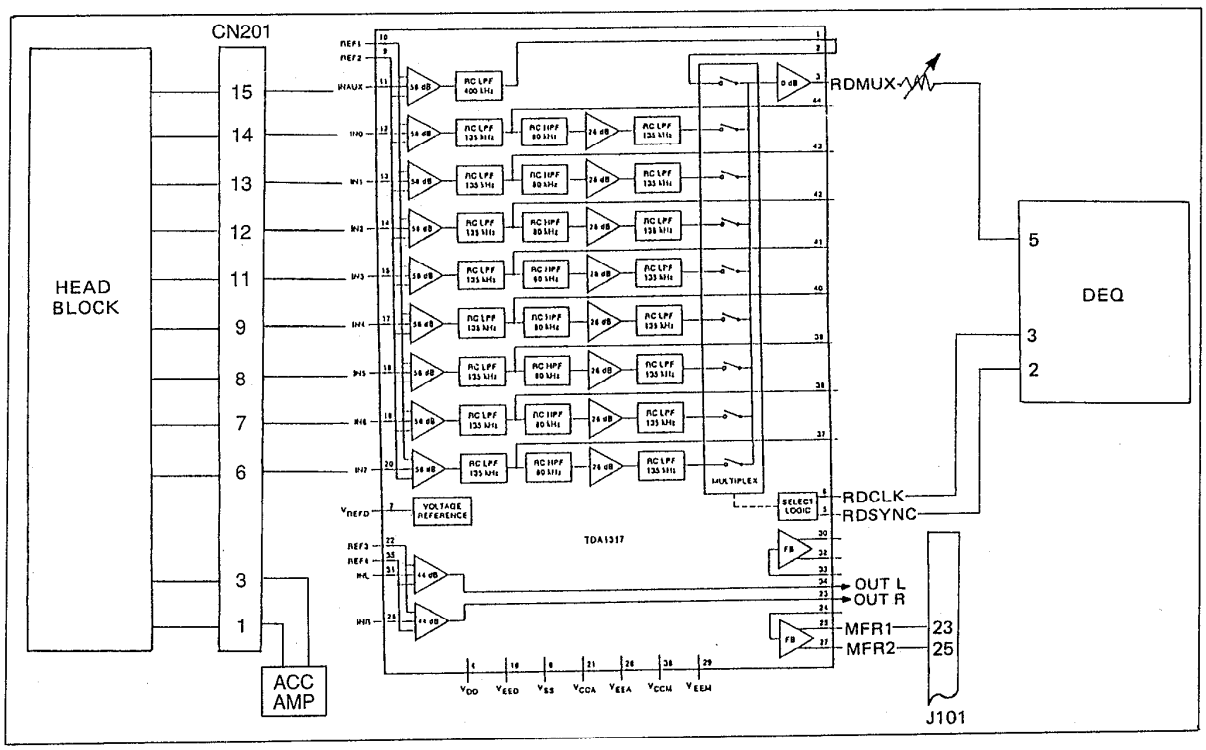


Fig. 4

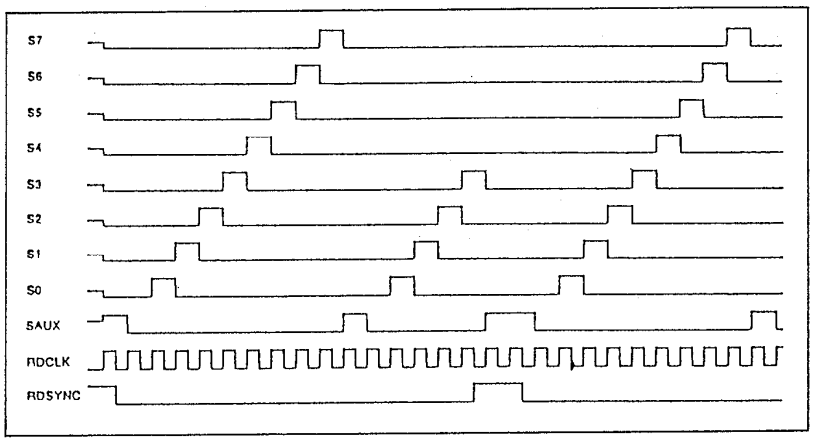


Fig.5 Multiplexer Sequence Timing

6. DEQ/Digital Equilizer

FUNCTIONAL DESCRPTION

Operational Modes

DEQ operating modes are programmed via the LT interface:

NORMAL

- AD conversion
- demultiplexing
- equalization
- zero crossing

In this mode the DEQ (SAA2051) performs the equalization and slicing of the eight data channels and the auxiliary channel. The eight data channels have a bit-rate of 96 Kbit/s while the auxiliary channels has a bit-rate of 12 Kbit/s.

The DEQ (SAA2051) input is a time-multiplexed analogue signal from the Read Amplifier. The signal contains ten time slots, of which nine are used. The Read Amplifier and the DEQ (SAA2051) synchronize with the RDCLK and RDSYNC signals generated by the DEQ (SAA2051).

Following A/D conversion and demultiplexing the nine channels are equalized. The encoding of the equalizing coefficients (12 per channel) are not fixed and must be loaded via the LT interface before operation.

The nine equalized output signals are up-sampled by a factor of 10 with the resulting signals fed to the slicer. The slicer output is applied to the DDSP (SAA2041).

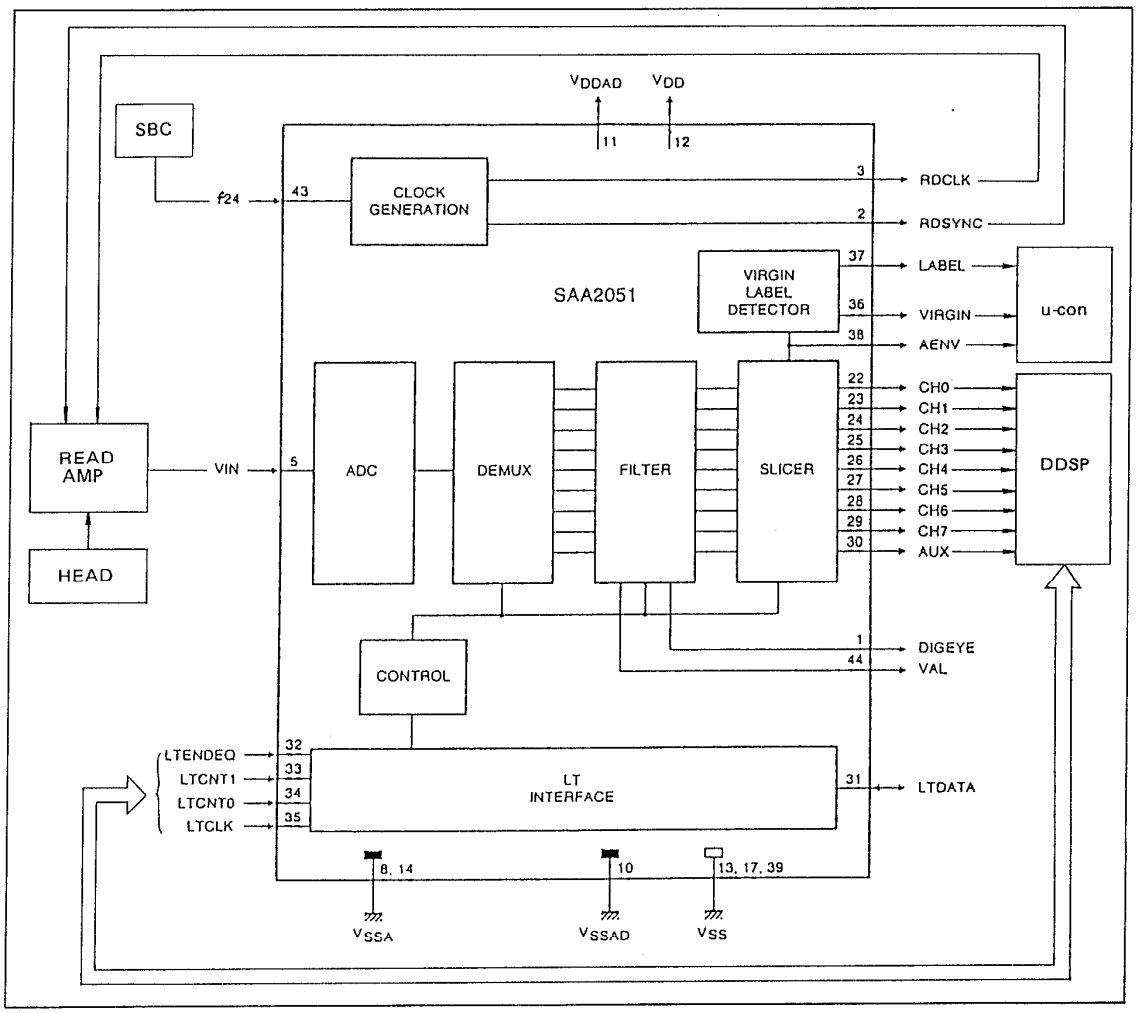


Fig. 6

READ AMPLIFIER INTERFACE

The interface between the Read Amplifier and the DEQ (SA2051) consists of three signals:

VIN from Read Amplifier to DEQ (SAA2051); time multiplexed data

RDSYNC from DEQ (SAA2051) to Read Amplifier; synchronization between Read Amplifier multiplexer and DEQ demultiplexer

RDCLK from DEQ (SAA2051) to Read Amplifier; data clock for Read Amplifier multiplexer

The multiplexed VIN output of the Read Amplifier; changes to another channel at the rising edge of RDCLK. RDSYNC synchronizes the Read Amplifier VIN output: If RDSYNC is HIGH, the rising edge of the RDCLK will select the AUX channel.

Figs. 7 and 8 show the relation ship between DEQ (SAA2051) and the Read Amplifier.

Table 1 Dependency of Read Amplifier on Operational Mode

OPERATIONAL MODE	RDSYNC	RDCLK
normal	YES	YES
test	YES	YES
search	HIGH	YES
OFF	HIGH	HIGH

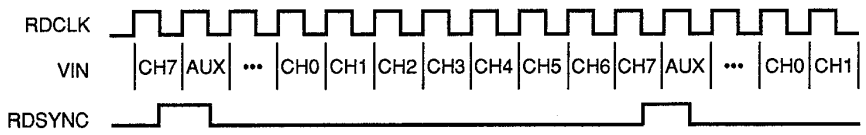


Fig. 7 Signals on Interface Between Read Amplifier and DEQ (SAA2051)

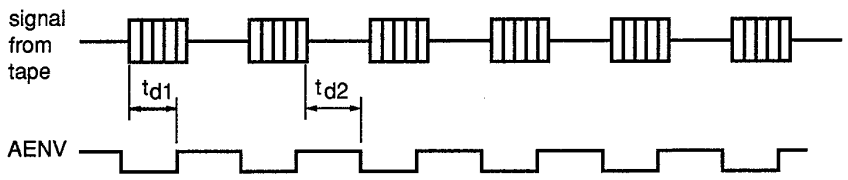


Fig. 8 $t_{d1} = t_{d2}$ = between 0.5 and 1.0 Auxiliary Block Lengths

LABEL AND VIRGIN DETECTION INTERFACE

When the DCC player is in its search mode, the tape is fast-wound while the head retains tape contact. The DEQ (SAA2051) can be made to operate in the search mode and the information will be read from the auxiliary tape track.

The following three signals are generated:

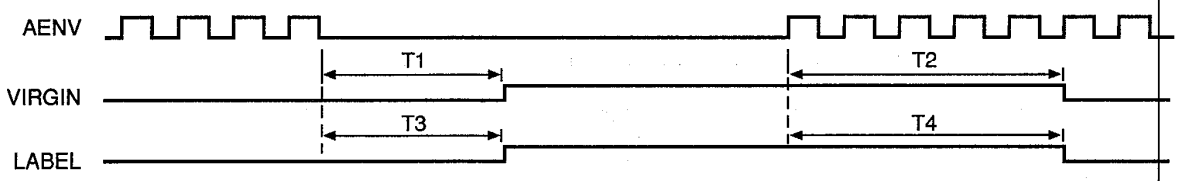
- LABEL label detection (HIGH if label is detected)
- VIRGIN virgin tape detection (HIGH if virgin tape is detected)
- AENV Alternating envelope (sliced envelope)

AENV, LABEL and VIRGIN are disabled in normal off modes. LABEL, VIRGIN and AENV are LOW. AENV, LABEL and VIRGIN are enabled when the DEQ (SAA2051) is in search mode.

The device detects the envelope AENV of the auxiliary track at search speeds between 3 and 50 times normal speed. If AENV is continuously HIGH (label detection), LABEL will be HIGH.

When AENV is continuously LOW (virgin tape detection) VIRGIN will be HIGH.

Figs. 9 show the relationship between AENV, VIRGIN and LABEL.



T3 = between 4 and 12 auxiliary blocks.
T4 = between 4 and 12 auxiliary blocks.
T1 = T2 = between 4 and 12 auxiliary blocks.

Fig. 9

LABELED TAPES SPEED CALCULATION

When the DCC player is in its search mode, the tape speed increases. LABEL informationis encoded throughout its length. To examlne the length of a label, the tape speed must be known. In search mode the DEQ (SAA2051) assesses the speed of labelled tapes. The microcontroller obtains this information via the LT-interface.

The speed information is encoded in the three variables:

- SVF Speed Validation Flag (HIGH if invalid)
- SC (4 ... 0) Speed Counter
- SR (1 ... 0) Speed Range

Search speed 2 ——

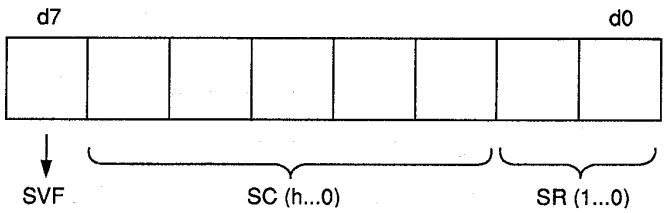


Fig.10 Tape Speed Data Format

7. DDSP/Digital Drive Signal Processing

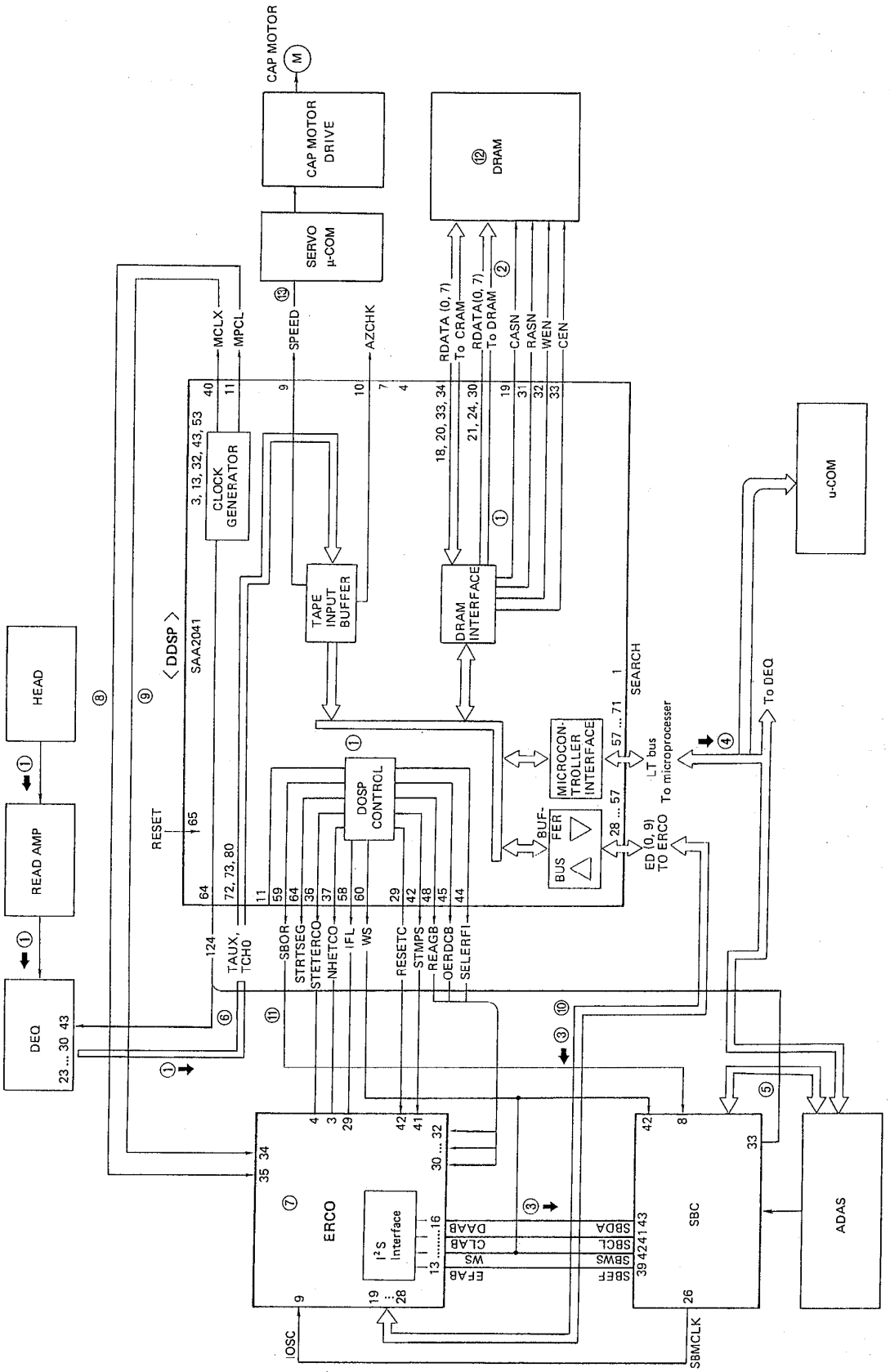


Fig. 11

DDSP/Digital Drive Signal Processing

Performing digital signal processing within the DCC (Digital Compact Cassette) system, the DDSP (Digital Drive Signal Processing; SAA2041) device pocesses control, address generation and data formation functions within the system. Its main functions include control of the ERCO (SAA2031) device together with the processing of data from the DEQ (SAA 2051).

Functional Description

Modes

The DDSP (SAA2041) can be operated in any one of three modes:

DPAP (Data Play-back and Aux Play-back)

The DDSP synchronizes to the WS (I^2S-interface word select) signal.

DPAP Mode (DECODE) ←

In the data play-back/aux play-back mode, the equalized data from the mine tape tracks are ←① fed to the DDSP (SAA2041) which recovers and demodulates the channel bit streams and stores ←② them in the DRAM.

The DDSP (SAA2041) controls the flow of data to and from the ERCORR section of the ←③ ERCO (SAA2031) device. When all the data has been processed the DDSP (SA2041) sends the sub-band data via the I^2S-interface in the ERCO (SAA2031) to the SBC (SAA2021).

The AUX and SYSINFO data can be trans- ←④ ferred to the microcontroller via the LT interface.

Clock Interfacing

The 24.576 MHz clock input is fed directly from the SBC (SAA2021) pin 124. ←⑤

Interfacing the DDSP (SAA2041) to the Digital Equalizer.

Nine lines (TCH0...TCH7 and TAUX) connect the DDSP to the DEQ (SAA2051). ←⑥

DPAR Mode

When the system is set to the data play-back mode, the microprocessor must read SYSINFO from this device.

Equalized channel data from the 8 data carrying tracks are fed to the DDSP for recovery and demodulation. The DDSP (SAA2041) stores this data in the DRAM.

Interfacing the DDSP (SAA2041) to the ERCO (SAA2031)

The ERCO (SAA2031) provides the Reed ←⑦ Solomon error correction encoding and deconding for the DCC system and I^2S-bus interfacing to the SBC (SAA2021).

The MCLK line provides the 6.144 MHz clock ←⑧ signal connecting to the MCLK input of the ERCO (SAA2031) device.

The MPCL line provides the 3.072 MHz clock ←⑨ phase reference signal which connects to the MPCL input of the ERCO (SAA2031) device. (This signal is not necessarily in phase with the WCLOCK line).

Data is transferred between the DDSP ←⑩ (SAA2041) and the ERCO (SAA2031) via a 10-bit parallel bus (ED0-ED9).

Interfacing to the SBC (SAA2021)

Two DDSP (SAA2041) output signal (SBDIR and URDA) supplement the I^2S-interface connection from the ERCO (SAA2031) to the SBC (SAA2021).

SBDIR controls the direction of data transfer ←⑪ on the I^2S-interface between the SBC (SAA2021) and the ERCO (SAA2031): SBDIR = HIGH.

Interfacing the DDSP (SAA2041) to the DRAM

The DDSP operates with a 64 K-words × 4-bit Dynamic RAM in page mode with a 80 ns to ←⑫ 120 ns row access time. Refreshing of the DRAM will be within 4 ms. Transfers to and from the nibale DRAM occur in bursts of 3 nibbles.

Interfacing the DDSP (SAA2041) to the Capstan Motor

The SPEED signal is a pulse width modulated control output for phase regulating, via a filter, the speed of the CAPSTAN in the tape deck; hence the tape speed. ←⑬

In the mode DRAR or if the NOMSPD detting is 1, the speed cycle is set to a nominal of 50% duty cycle. In modes DPAP and DPAR, if the NOMSPD setting is 0, the duty cycle increases in a linear fashion to drive the capstan faster; if the tape travel is too slow, or vice versa.

A 0% duty cycle results from a type input that arrives too early, and a 100% duty cycle occurs from one that arrives 2 tape blocks too late. The normal operating range is ± 1.2 blocks. Operation outside this range is not recommended.

The output is from a phase detector with a sensitivity (kd) $5/2\pi$ volt/red and a measuring repetition frequency of 47 Hz. The output frequency is 24 kHz with a duty cycle between 0 and 100%. When the tape speed deviates more than 10% from nominal, the phase detector holds its last value.

8. ERCO/Error Correction

The timing relationship between DATA0-DATA7, FLAG1, FLAG2, OERRCB, READB, SELERFI, MPCL and the MCLK are given in Fig. 13 Data transfers to or from the ERCO (SAA2031) via the Data Bus must occur an even number of MPCL periods following STMPB.

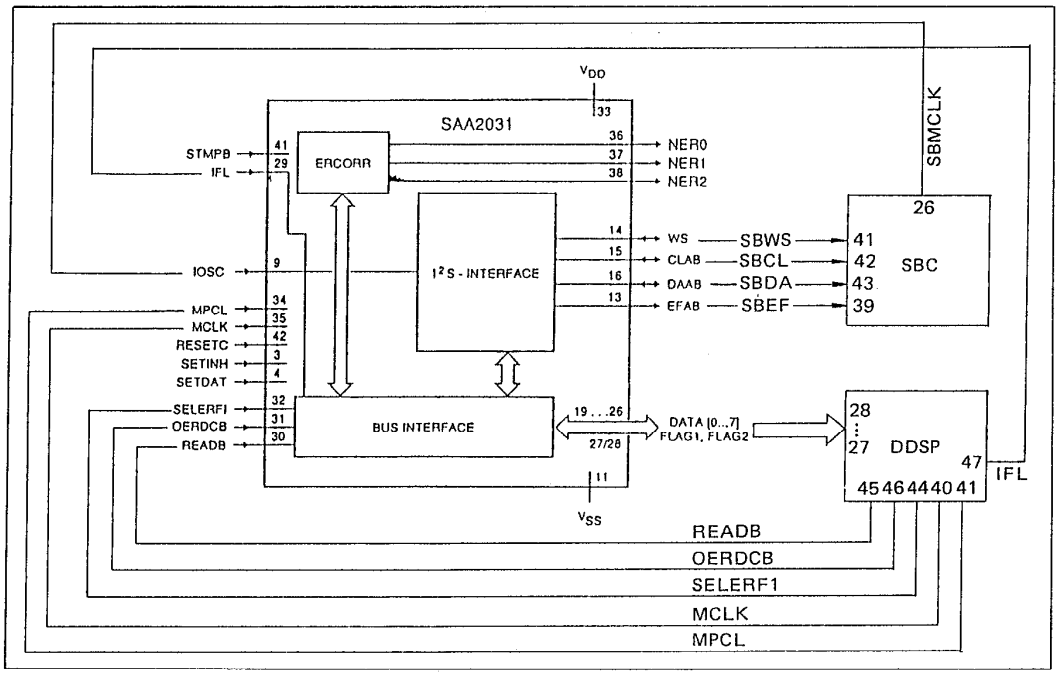


Fig. 12

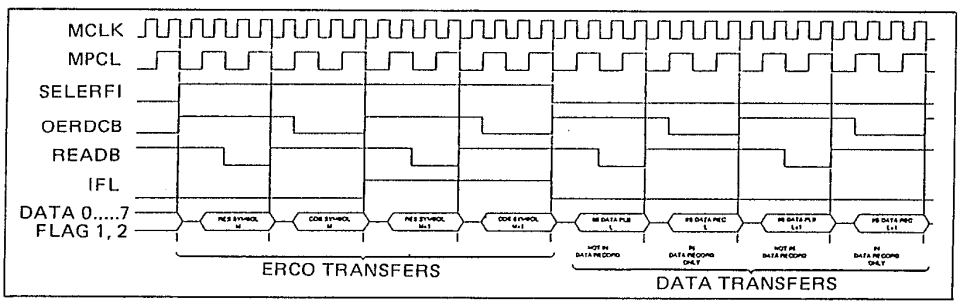


Fig. 13 Rata Transfer Between DDSP and ERCO

9. ADAS/Adaptive Allocation and Scaling

The PASC system calculates the masking power of the sub-band signals and adds the masking threshold. Sub-band signals with power below this threshold denote information to be discarded.

Non-masked signals are coded using floating point notation in which a mantissa corresponds in length to the difference between peak power and masking threshold. The process is repeated for every PASC frame and is known as the Adaptive Allocation of the avaliable capacity.

In the playback mode (FDIR = HIGH, pin 37) the ADAS will take samples from FDAC (pin 33). These will be presented on FDAF (pin 34) after a delay of 160 SWS periods. Although settings and status information will be exchanged between the LT interfaces of microcontroller and SBC (SAA2011) will be unaffected except for accepting the ready-to-receive bit from the SBC (SAA2021).

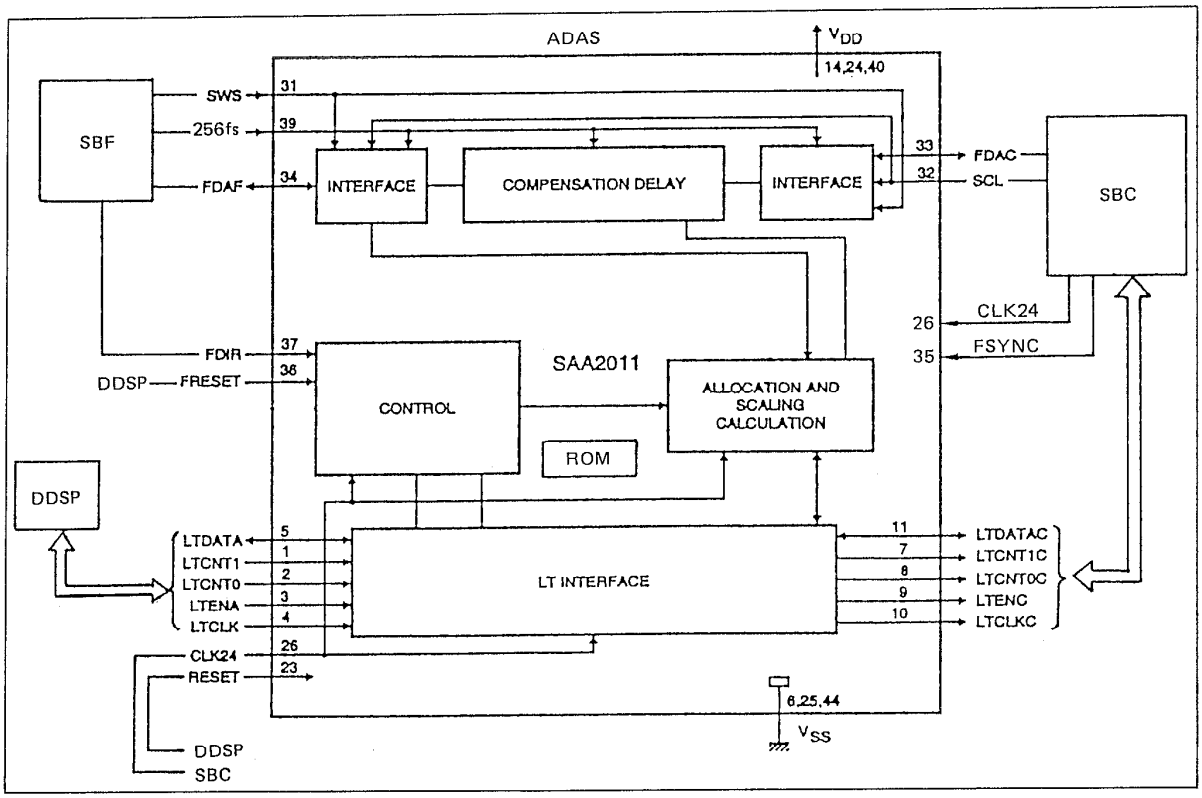


Fig. 14 Block Diagram

(Filtered-I²S-Interfaces)

Interfaces with the SBF (SAA2001) filters and SBC (SAA2021) consist of the following signals:

The (Filtered)-I²S-Interface:

SWS	Input	Word selection	fs
SCL	Input	bit-clock	64 fs
FDAF	bi-dir	filtered data to/from SBF (SAA2001)	
FDAC	bi-dir	filtered data to/from SBC (SAA2011)	
FSYNC	input	filter synchronization	fs/32

256 fs must be provided as sytem clock. This frequency is used by the interfaces with the SBC (SAA2021) and SBF (SAA2001) filters.

The frequency of the SWS signal (pin 31) is equal to the sample frequency fs Bit-clock SCL (pin 32) is 64 times the sample frequency; thus each SWS period contains 64 data bits, 48 of which are actually used in data transfer. The half period during which SWS is 0 is used to transfer Left-channel information while that during which it is 1 permits transfer of Right-channel data.

The 24-bit samples are transferred with the most significant bit first. This bit is transferred during the bit-clock period, one bit-time after the change in SWS.

FSYNC signal is provided for the purposes of synchronization and indicates the portion of the SWS period during which the samples of sub-band 0 are transferred.

Fig. 16 shows the relationship between FSYNC and SWS0 data transfer period.

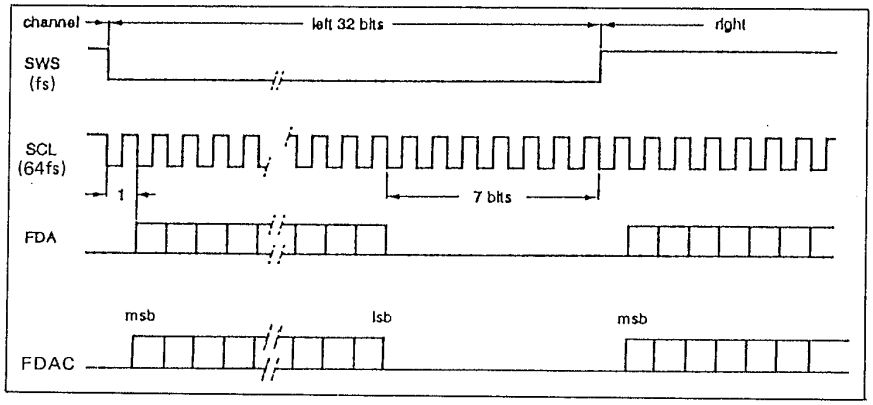


Fig. 15 Format for Transferring Filtered Data

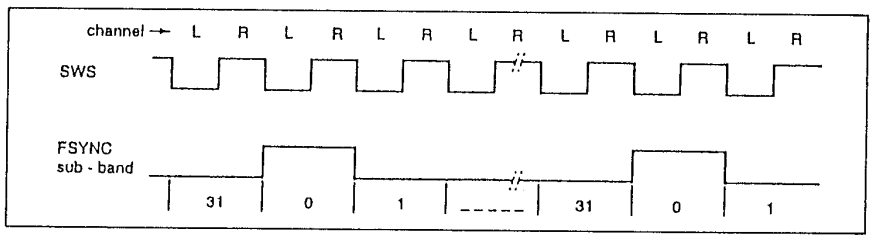


Fig. 16 FSYNC Related to SWS 0 Data Transfer Period

10. SBC/(Sub Band/Decoder)

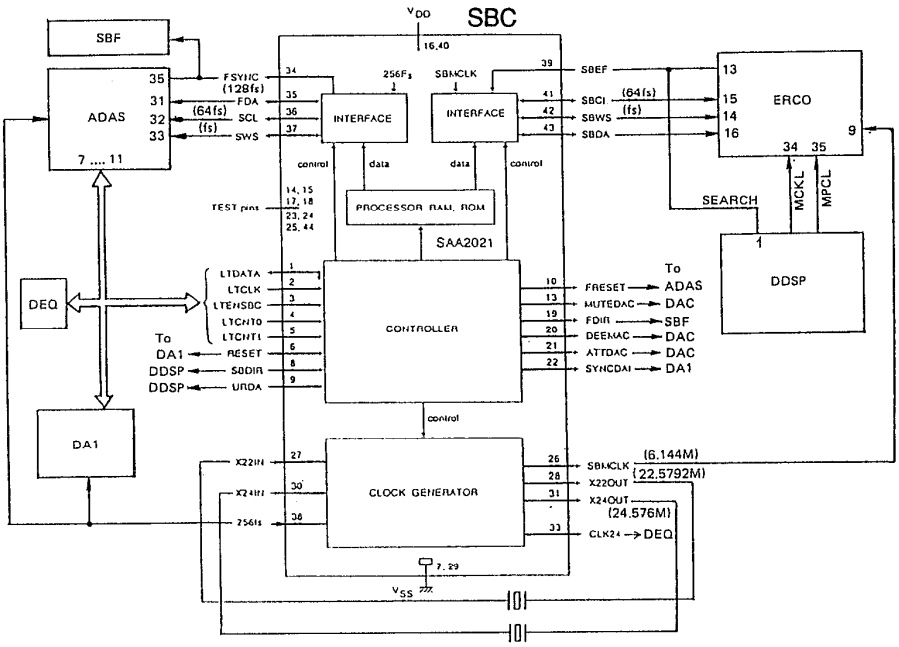


Fig. 17

Decoding

All essential information (synchronization, system information, scale factors and encoded sub-band samples) are conveyed by incoming data.

Deconding is repeated for every frame.

After sync and system information, allocation data and the scale factors are used to correctly fill the scale factor array.

This is followed by a process of multiplication to provide de-quantization and de-scaling of the PASC samples. The decoded sub-band samples are then sent to the sub-band filters.

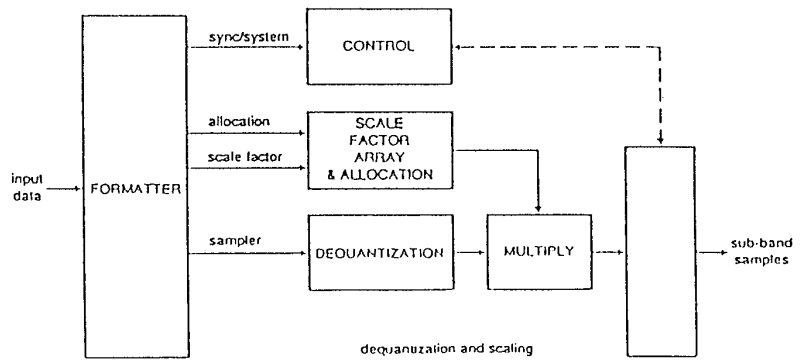


Fig. 18 Decoding mode

Allocation Information (LTCNT1 = 0, LTCNT0 = 1) 16 complete transfers of 16-bits are required to provide the allocation table to the SBC (SAA2021). The intermal prograv of the SBC (SAA2021) must become synchronized with this data.

Allocation information transfer is completed by sending settings information. The ADAS (SAA2011) device performs this function automatically.

The 4-bit allocation information unit contains the number of bits allocated to the sub-band, MINUS 1. A value of 0000 indicates no bits are allocated to a sub-band. Value 1111 is not used.

With stereo encoding the channels are indicated with L and R (Left and Right).

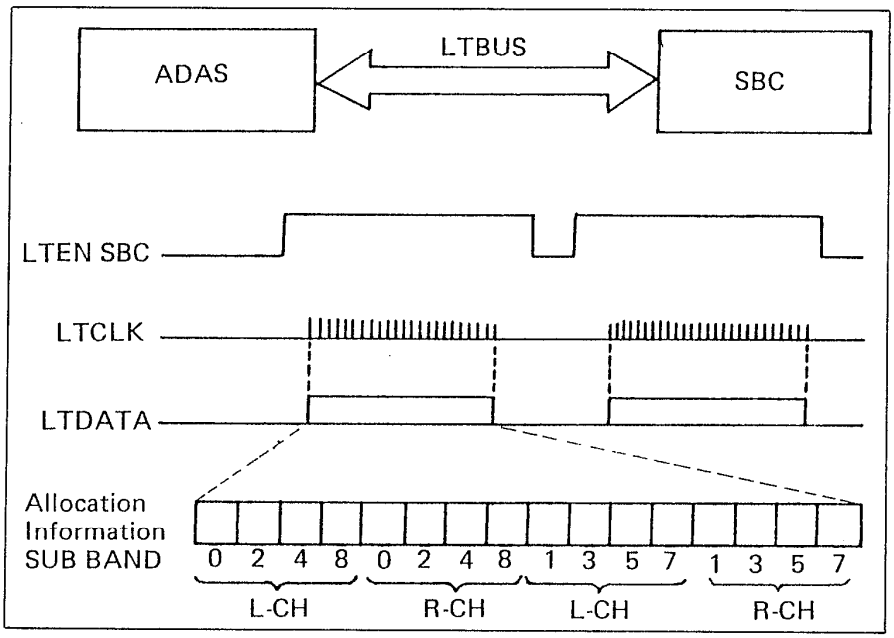


Fig. 19

Table 2 Modes and Source Signals

LTCNT1	LTCNT0	Mode	From	To	Transfer o.
0	0	ext settings	ADAS	SBC	8-bits
0	1	allocation	ADAS	SBC	16 × 16-bits
1	0	settings	ADAS	SBC	16-bits
1	1	status	SBC	ADAS	8 or 16-bits

Allocation information 4-bit units.

msb			bits			lsb	channel		sub-band
A15	–	A14	–	A13	–	A12	L	or	I 0, 2, 4, 8
A11	–	A10	–	A9	–	A8	R	or	II 0, 2, 4, 8
A7	–	A6	–	A5	–	A4	L	or	I 1, 3, 5, 7
A3	–	A2	–	A1	–	A0	R	or	II 1, 3, 5, 7

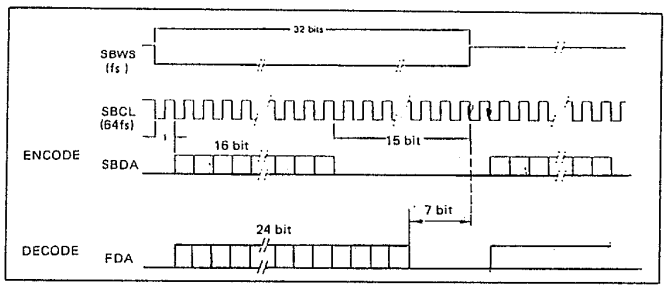


Fig. 20 Transferning Sub-Band Coded Data to and from the SBC (SAA2021)

Each period of SBWS contains 64 data-bits of which 32 are used to convey data. The half-period during which SBWS is 0 is used to transfer the first 16 bits (0–15) of a sub-band slot. The remaining half-period during which SBWS is 1 carries the remaining 16-bits (16–31). Thus one period of SBWS corresponds with one slot of sub-band signal.

Bits 0 and 16 are transferred in the same bit-clock period, one bit-time after the change in SBWS. Both SBWS and SBRA change state during the negative edge of SBCL.

Decoding mode

SBCL, SBWS and SBDA are produced based on SBMCLK, by an external source.

Microcontroller Interface

The SBC (SAA2021) has an interface connection to the serial interface of a microcontroller:

LTCLK	input	bit-clock
LTDATA	bi-dir	data
LTCNT0	input	control line 0
LTCNT1	input	control line 1
LTENSBC	input	enable

The SBC (SAA2021) microcontroller interface is enabled only if LTENSBC (pin 3) is 1. Information to or from the SBC (SAA2021) is conveyed in serial 8 or 16-bit units whilst the type of information is controlled by LTCNT0 (pin 4) and LTCNT1 (pin 5). A transfer begins when the ADAS (SAA2011) activates the control lines for the required action. LTENSBC (pin 3) is set to 1. The SBC (SAA2021) determines its required action and prepares to transfer data.

Upon the supply of LTCLK (pin 2) from the ADAS (SAA2011) device, data is transferred to or from the SBC (SAA 2021) in units of 8-bits. 16-bit transfers are conveyed as two 8-bit units during which LTENSBC remains at 1.

During the transfer of 8-bit units, the least significant bit is first to be transferred. When 16-bit units are transferred, the most significant 8-bit unit is the first to be sent.

11. SBF/Sub Band Filter

The SBF (SAA2001) can function in encoding (FDIR = L) or decoding (FDIR = H) mode.
In encoding mode, the broad-band audio data from SDA (pin 30) is split into 32 sub-band signals. The sampling frequency, f_2, of the broad-band audio data is reduced to $f_2/32$ for each sub-band signal. The sub-band signals are transferred with the FDA signal as a sequence of one sample per sub-band. The sample for sub-band 0 appears on pin SDAT when FSYNC = H.

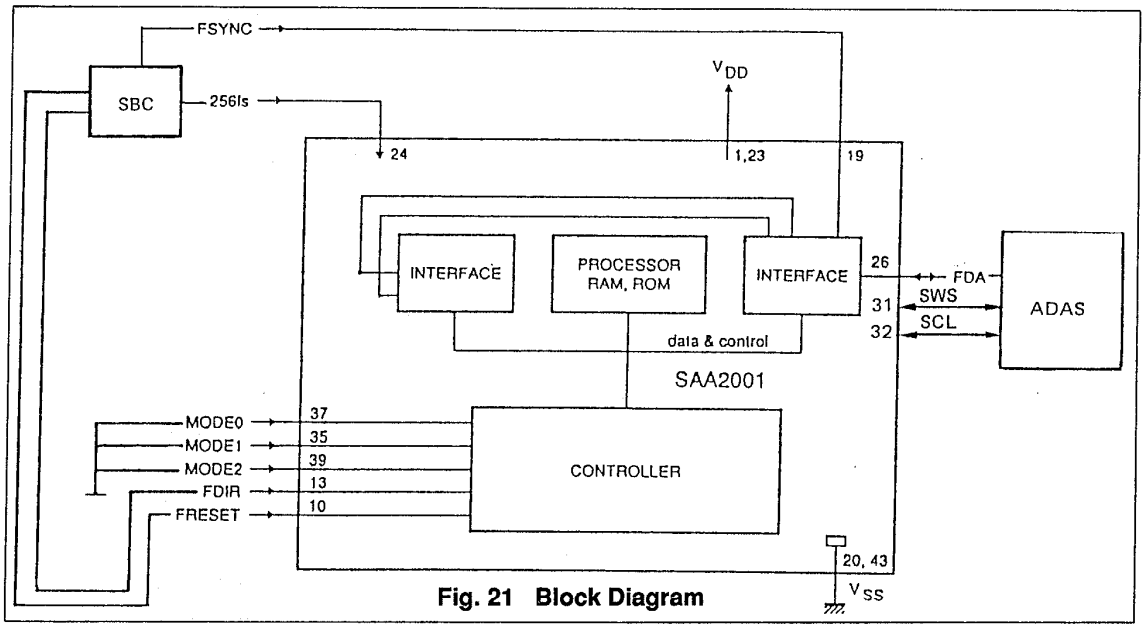


Fig. 21 Block Diagram

Encoding

Digital audio source signals from an I²S-interface are filtered by the SBF (SAA2001) device into the 32 sub-band signals for application to the Filtered-I²S-interface.
Input samples have a maximum of 18 significant bits in two's complement notation. If a larger quantity is provided to the interface only the most significant 18 bits are used in the calculation process.
Sub-band samples are represented using 24-bit two's complement notation.

Decoding

The SBF (SA2001) devices reconstruct the digital broadband audio signal from the 32 sub-band signals supplied via the filtered - I²S-interface by the SBC (SAA2021). This function is the complete inverse of the encoding function.

Table 1 SBF Bandwidths Related to Sampling Frequencies

SAMPLING FREQUENCY	SAMPLING FREQUENCY	SUB-BAND
Broadband signal	Sub-band signals	Bandwidth
48 kHz	1500 Hz	750 Hz
44.1 kHz	1378 Hz	689 Hz
32 kHz	1000 Hz	500 Hz

Mode Selection Pins

Three MODE selection pins (pins 35, 37, 39) designate the operating channel and the interface format for the broadband signal. With the PASC system, pins 35 and 37 are held at 0 (I^2S-interface mode). When the SBF (SAA2001) is used for decoding the RIGHT channel in a stereo system, pin 39 (MODE 2) is held at 1. For LEFT channel operation pin 39 is held at 0.

Operational Mode Control

SBF operation is controlled by FRESET and FDIR: FRESET causes a general reset.

FDIR indicates the direction of data flow.

FDIR = 1 playback mode

FDIR = 0 recording mode

When FDIR (pin 13) is 1, 32 sub-band channels digital audio data from the ADAS (SAA2011) or SBC (SAA 2021) device is fed into FDA (pin 26). It is combined into a single digital audio signal which emerges from SDAT (pin 30) as an OUTPUT to the D/A converter.

When FDIR (pin 13) is 0, digital audio INPUT data from the A/D converter flows through the device from SDAT (pin 30) and emerges as data contained in 32 sub-band channels at FDA (pin 26).

Broadband Signal Interface

The broadband signal interface consists of the following signals:

SWCK word (channel) selection input

SBCK bit-clock input

SDAT broadband bl-directional data

The SWS signal indicates the channel of the sample signal (either LEFT or RIGHT) and is equal to the sampling frequency fs.

Operating at a frequency 64 times of that used for sampling, the bit-clock dictates that each SWCK period contains 64 DDA data bits. Of these, a maximum of 36 are used to transfer data (samples may have a length up to 18-bits). Samples are transferred most significant bit first.

The most significant bit is transferred in the bit-clock period, one bit-time after the change in SWS state.

Fig.22 shows the transfer of SDA data.

The SBF (SAA2001) devices are synchronized to the SBC (SAA2021) by FSYNC (pin 19). This indicates the SWS period in which samples of sub-band 0 are transferred.

Fig.23 shows the relationship between SWS and FSYNC.

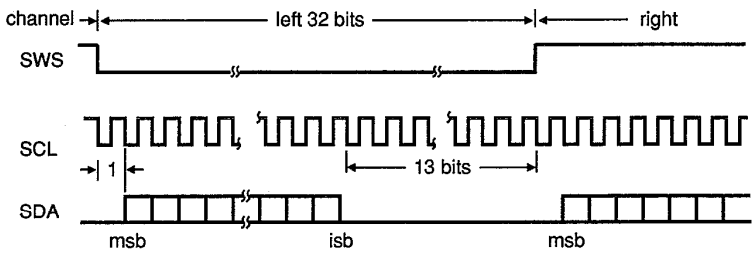


Fig. 22 Transfer of SDA Data

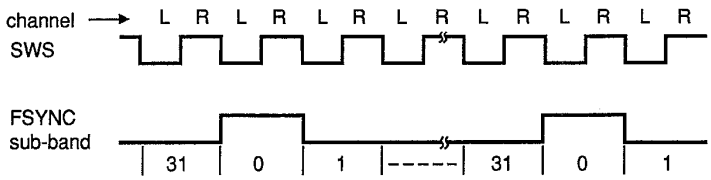


Fig. 23 SWS Related to Phase of FSYNC

12. D/F/Digital Filter and D/A/Digital Audio Convertor

FUNCTIONAL DESCRIPTION

In the TDA1545A (T) 32 current sources and one spare current source are continuously calibrated (Fig.24). The spare current source is included to allow continuous converter operation. The output of one calibrated source is connected to an 11 bit binary current devider, symmetrical offset decoding principle is incorporated and arranges the bit switching such that the zero-crossing is performed by switching only the LSB currents.

The TDA1545A (T) (CC-DAC) accepts serial input data format of 16 bit wordlength. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The input data format is shown in Fig. 25and Fig.26.

With a HIGH level on the WS input, data are placed in the left input register and with a LOW level on the WS input, data are placed in the right input register (Fig. 24). The data in the input registers are simultaneously latched to the output registers which control the bit switches.

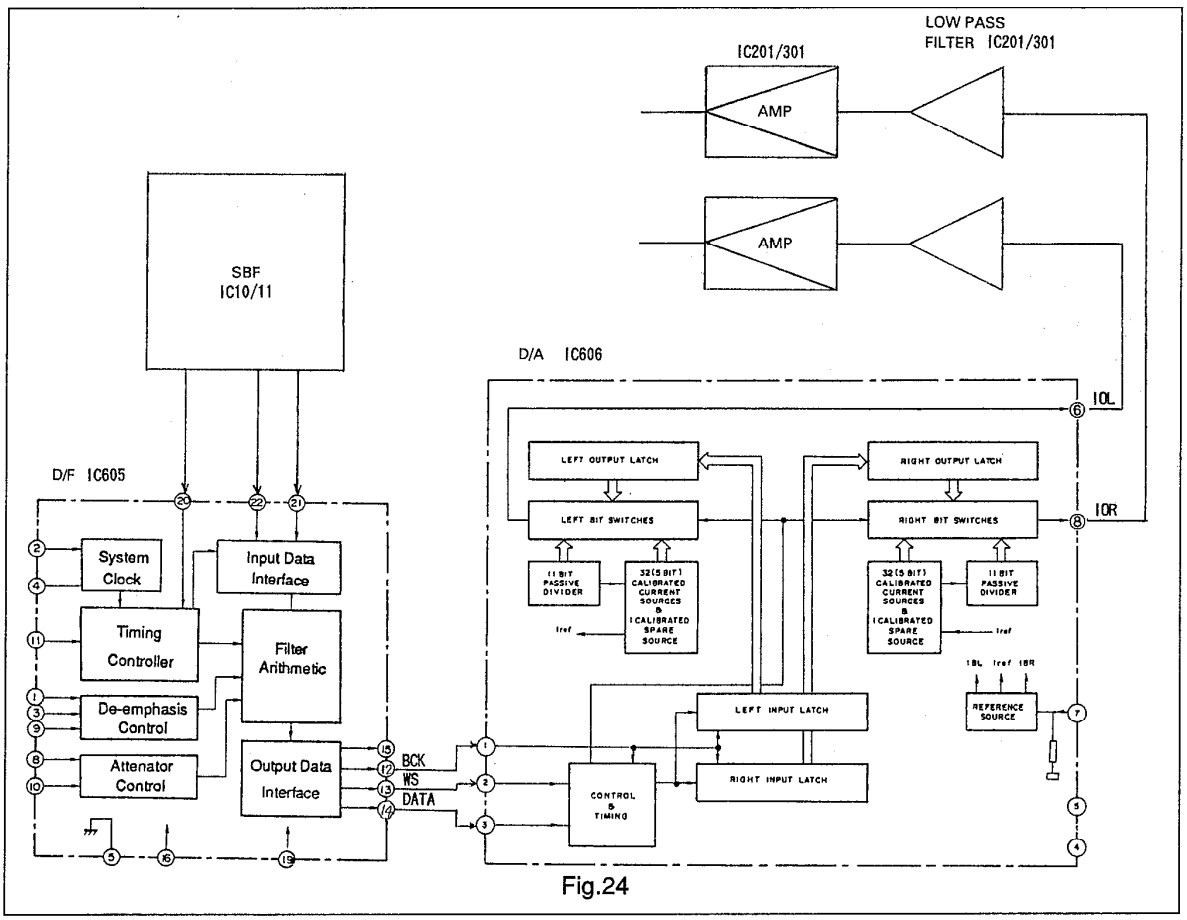


Fig.24

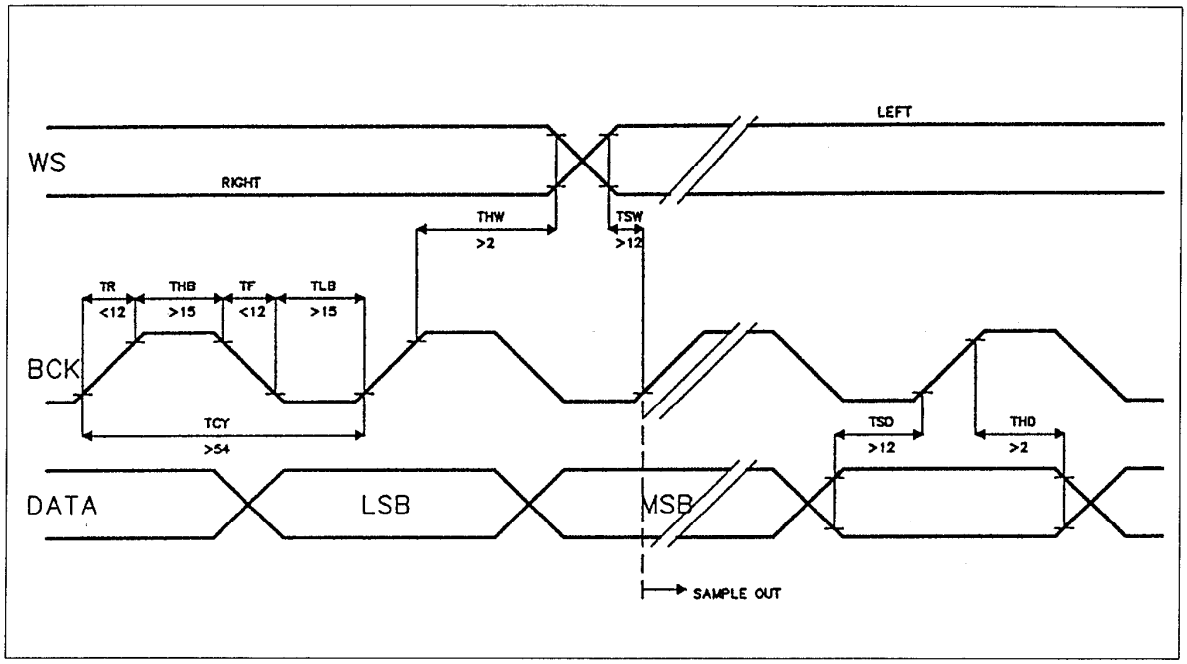


Fig. 25 Timing and input signals

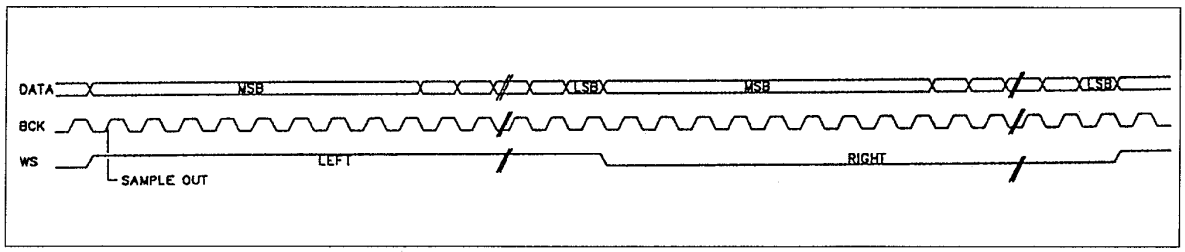


Fig. 26 Format of input signals

13. System Control Block

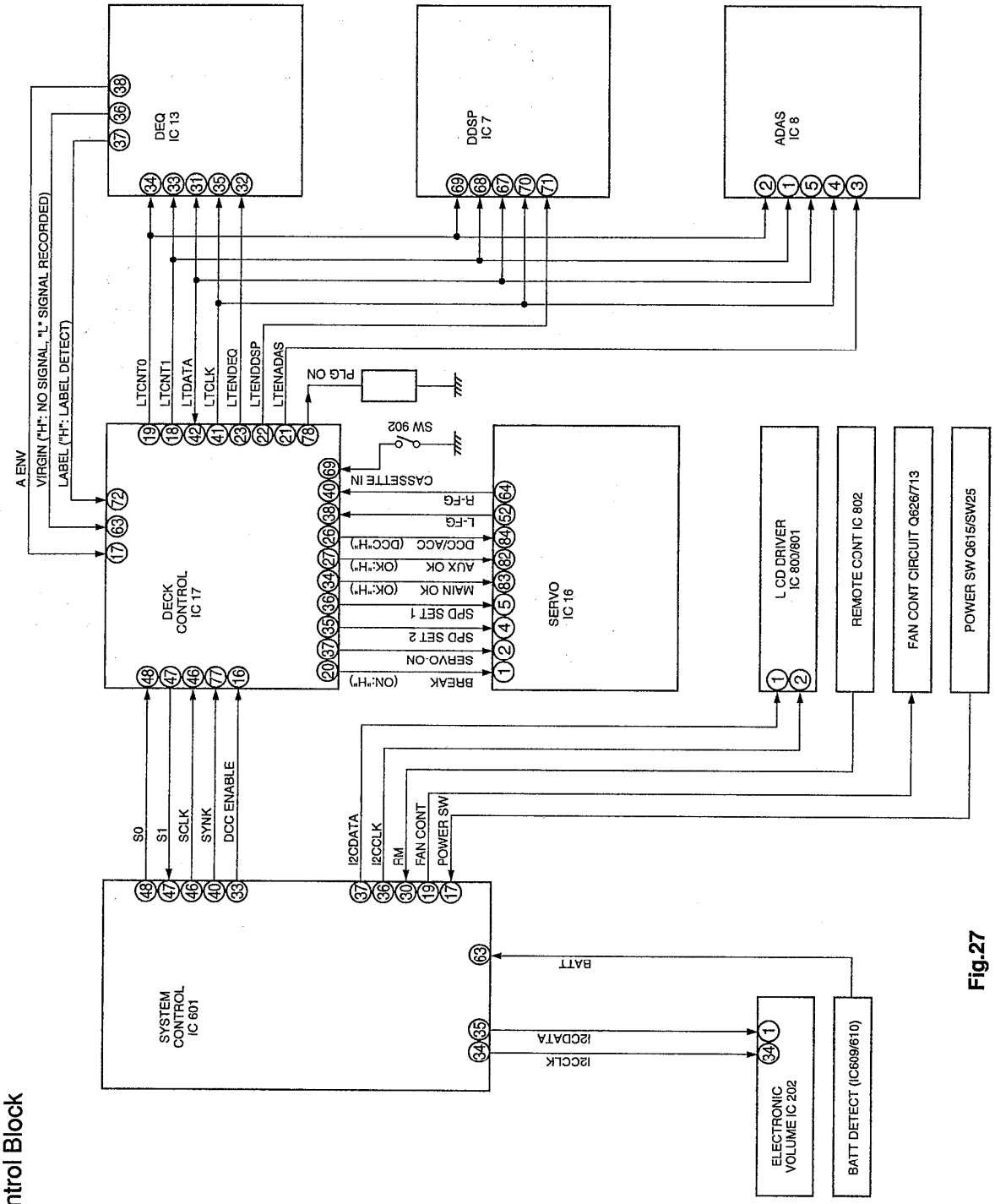


Fig.27

14. DCC Servo Circuit

Shown below is a playback servo block diagram of CAR DCC. The servo circuit uses a servo processor for 16-bit high speed operation and constitutes software digital servo mechanism.

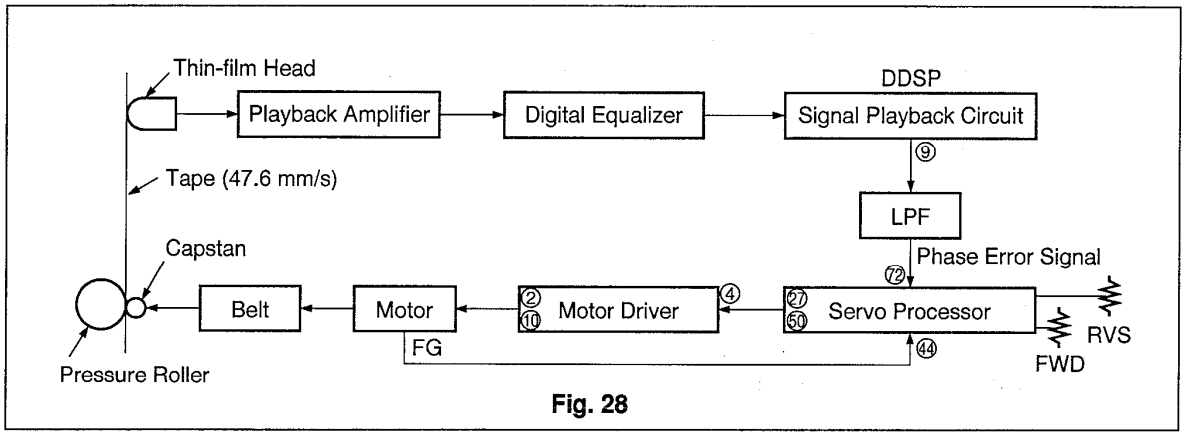


Fig. 28

DCC Playback

1. Capstan motor is controlled with clock oscillatio accuracy of servo processor (IC16) and tape is made to run at reference speed (4.76 cm/sec). Speed that differs by each mechanism is adjusted to reference speed independently in FWD and REV.
2. Signals played back from head are amplified at READ amplifier, and being equalized in waveform at digital equalizer, they are input to signal playback circuit (DDSP). Through check of phase difference between playback data and DDSP reference signals, they are output as phase error signals from DDSP. These signals are renewed every fourth block, modulated by PWM method, and are output as speed signals (at intervals of about 20 msec.).
   The following illustration shows the relationship between actual playback data deviation and speed signals.

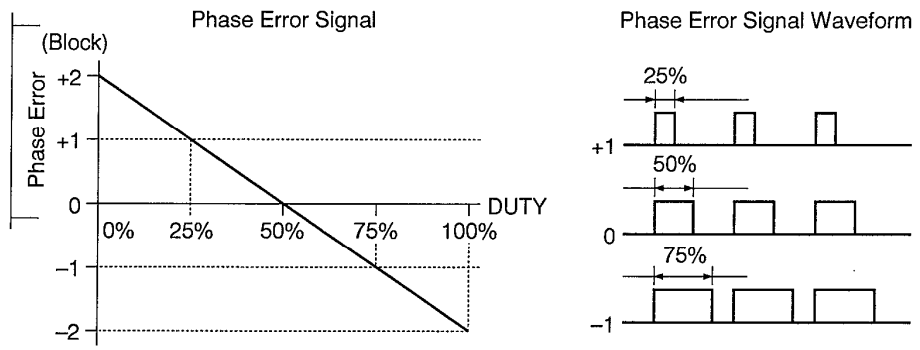


Fig. 29

Actual Servo Circuit Operation

The servo circuit operates during DCC playback as follows:

1. Start of capstan motor
   ① Supplies start signal as 8-bit serial data from DDSP IC7 pin ⑨ to servo processor/IC1.6 Pin ⑫.
   ② PWM signal output from IC16 Pin ㉗ is smoothed at LPF (R61, C39), and being made into DC, it is input to IC702A.
   ③ Reference voltage is input to IC702A, and through IC704 to Motor driver IC705. Motor starts to turn and rotates capstan.

2. Speed control by FG servo
   ① FG signal supplied from FG coil of motor (1 turn/30 pulses) is Being amplified by IC702B and IC703.
   ② FG signal input to servo processor/IC16 Pin ㊹ is compared every pulse with reference pulse and the result is output as PWM signal from Pin ㉗.

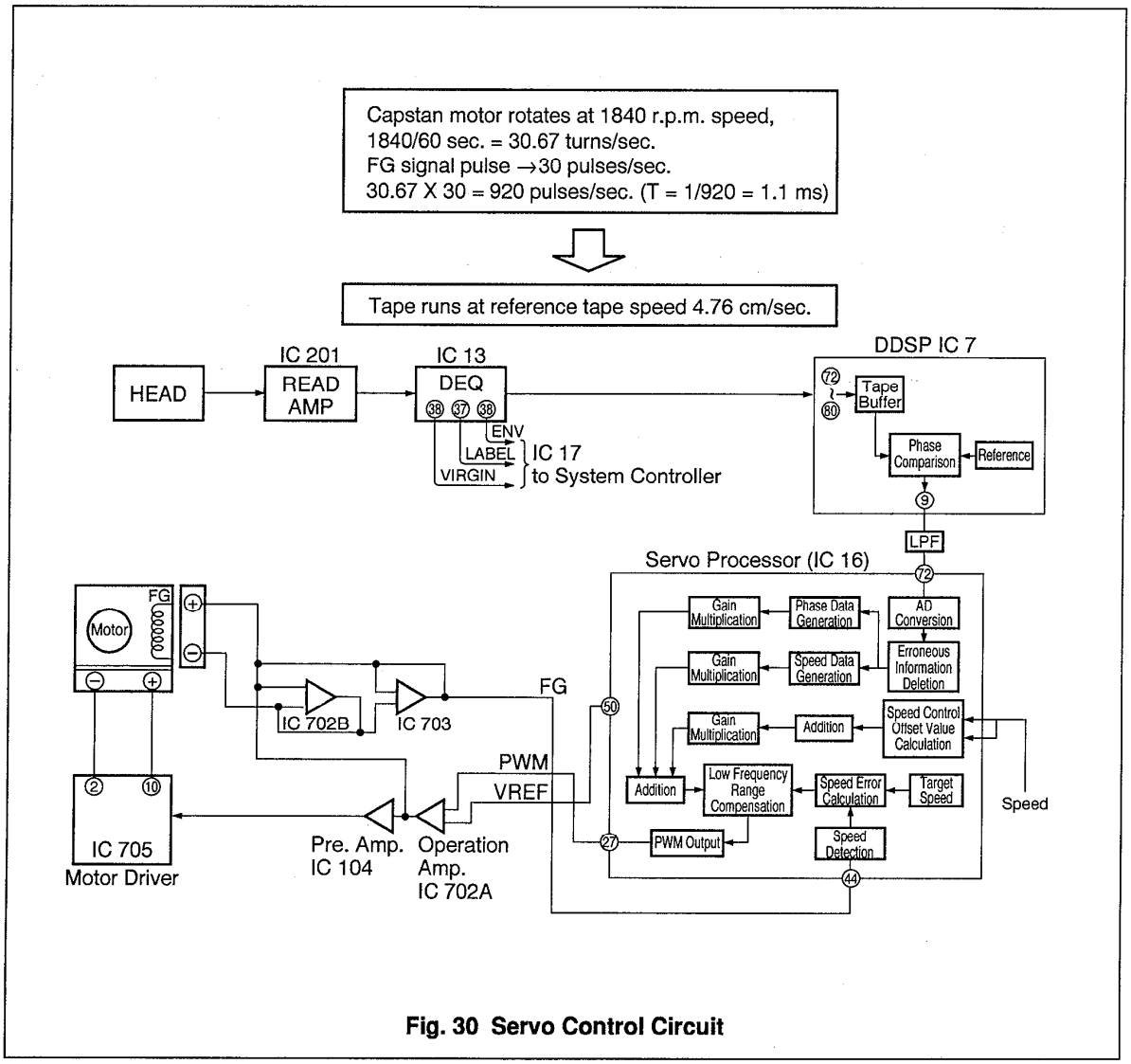


Fig. 30 Servo Control Circuit

15. DCC Search Operation

A variety of markers are recorded by use of AUX track at the beginning, end, music head, turning position, etc. Each marker is searched and when it is identified, stop, turn or heading action takes place according to the marker. Markers are classified into three by lengths of section (label section) where AUX data are recorded all over the AUX tape frame.

Where markers are not recorded (e.g. halfway of a piece of music, etc.), part with AUX data recorded and part with no recording are repeated alternately (non-label section).

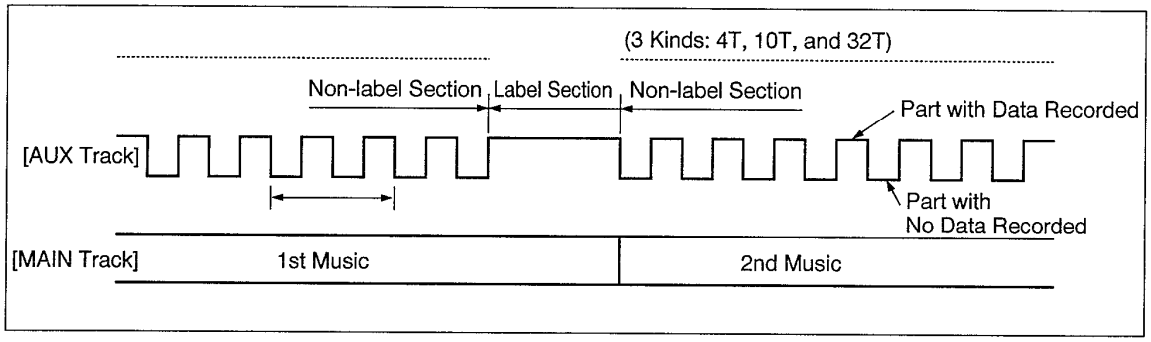
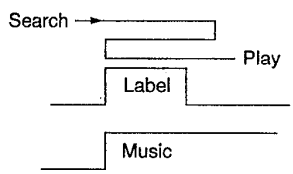
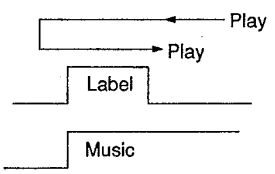
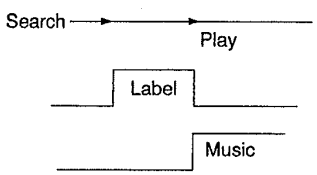
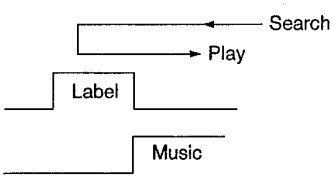


Fig. 31

Kinds of Markers classified for Different Lengths of Label Sections

4T → LEAD IN marker, LEAD OUT marker
16T → START marker
32T → REVERSE marker, etc.
} T:1 AUX frame

The table below shows recording position of start marker differing by tape (User Tape/Prerecording Tape) and mechanical operation during search:

	FWD Search	REV Search
User Tape		
Prerecording Tape		

DCC Search Operation

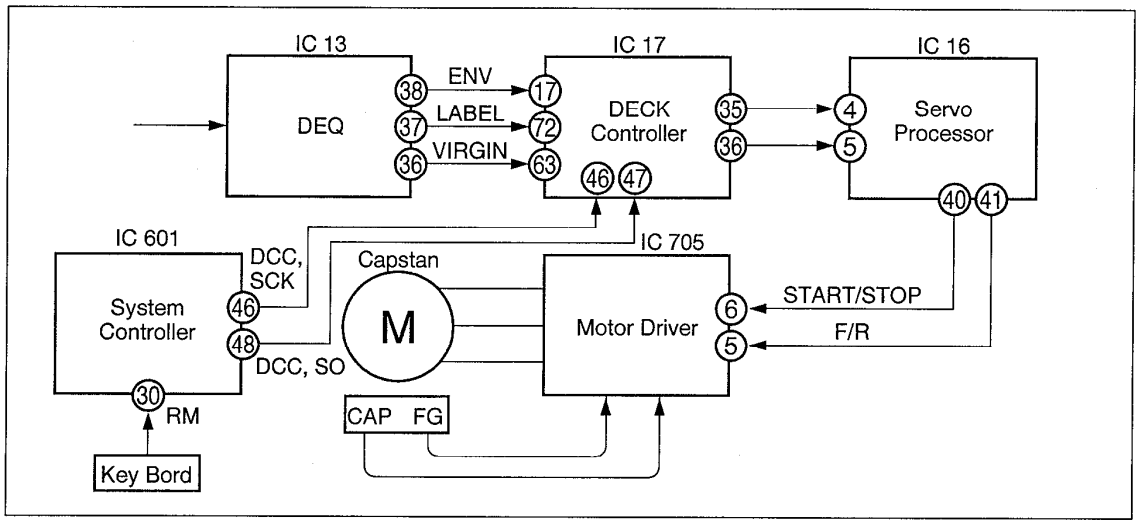


Fig. 32

DECK μ-CON OUTPUT		MOTOR CONDITION
(Pin 36) Pspd_set 1	(Pin 35) Pspd_set2	
L	L	NORMAL SPEED
H	L	0.5 TIMES SPEED
L	H	2 TIMES SPEED
H	H	STOP

(1) When the DCC SEARCH mode is selected, a SEARCH START command is input from the system controller IC601 Pin ㊽ to the deck controller IC17 Pin ㊼, and speed CONT signal is input from the servo processor IC16 Pin ④, ⑤.

(2) Thus the servo processor automatically works for speedup of the capstan motor following the steps shown in Fig. 33. (Rotational speed and time are programed previously. The speed is such as will permit detection of label even when the digital equalizer is at a high speed.)

(3) When the START marker is detected out of the AUX track during search, label information is input from the digital equalizer Pin ㊲ to the controller IC17 Pin ㉜, and a motor stop command is sent from Pin ㊽ to IC17 Pin ㊼.

(4) As this command is input from IC16 Pin ㊵, ㊶ to IC705 Pin ⑤, ⑥, the capstan is stopped temporarily (1 sec.).

(5) After that, a command for reverse rotation of motor is sent through DATA line from the DECK controller IC17. The reverse rotation time is from when the START marker is detected up to when the motor stops completely. In other words, the overrun portion is counted from the number of FG pulses from the capstan, and the motor is made to run in the reverse direction for the equivalent portion. Finally the motor is placed into the PLAY mode, and playback starts from the beginning of the program.

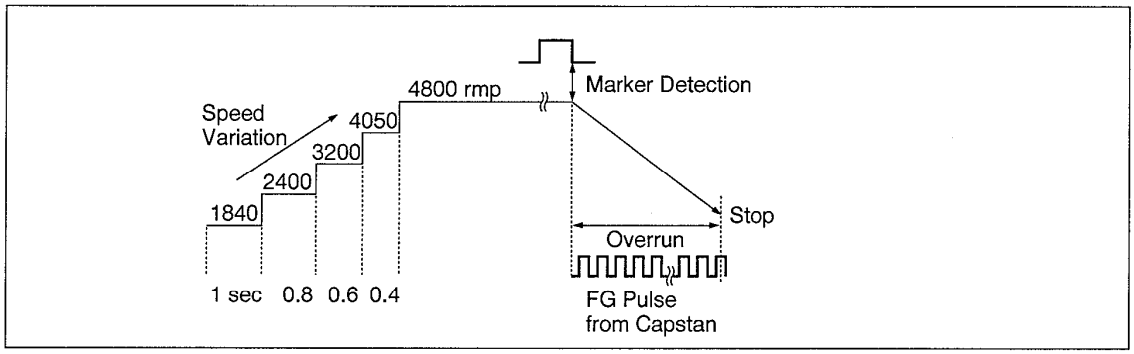

Speed
Variation
1840
2400
3200
4050
4800 rmp
Marker Detection
Stop
Overrun
1 sec
0.8
0.6
0.4
FG Pulse
from Capstan

Fig. 33

4. Troubleshooting Guide

Step 1 Power Supply Chart 87

•Check the power supply circuit

Step 2 Check Points in Mechanism 88

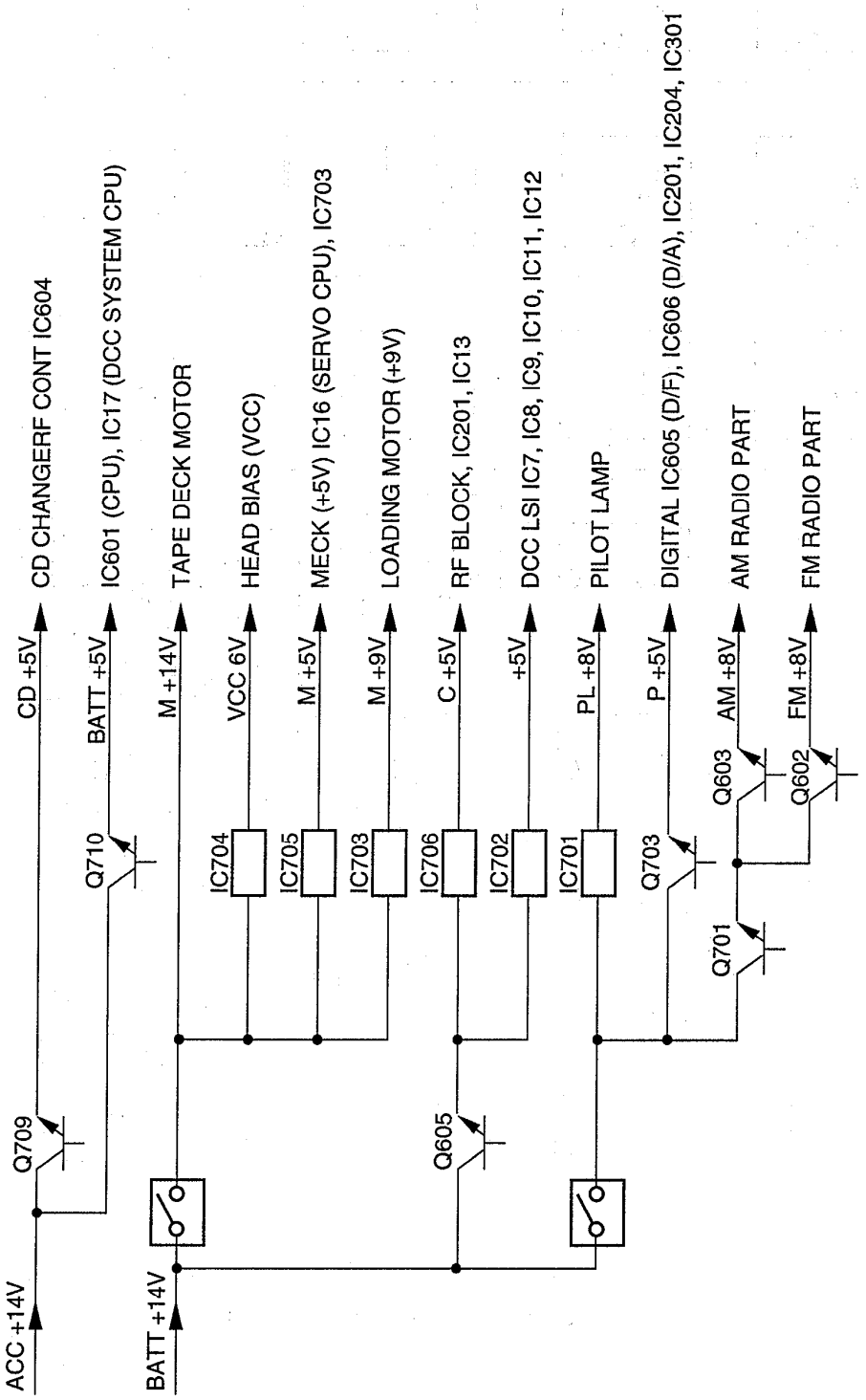
• Check the mechanism operations

Step 3 Check Points in Playback 89

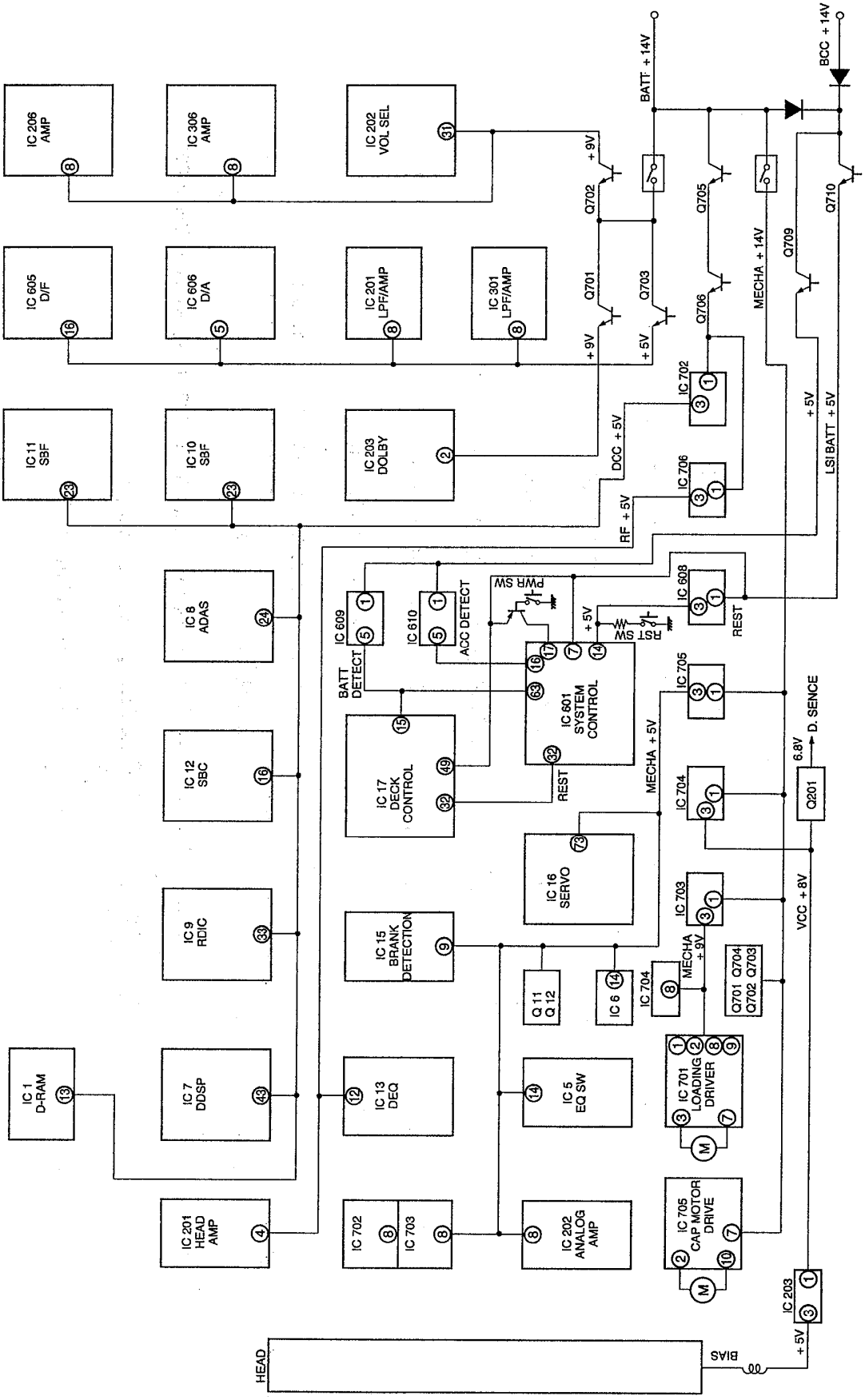
• Check the tape play operation

Step 4 Check Points by Phenomenon 90

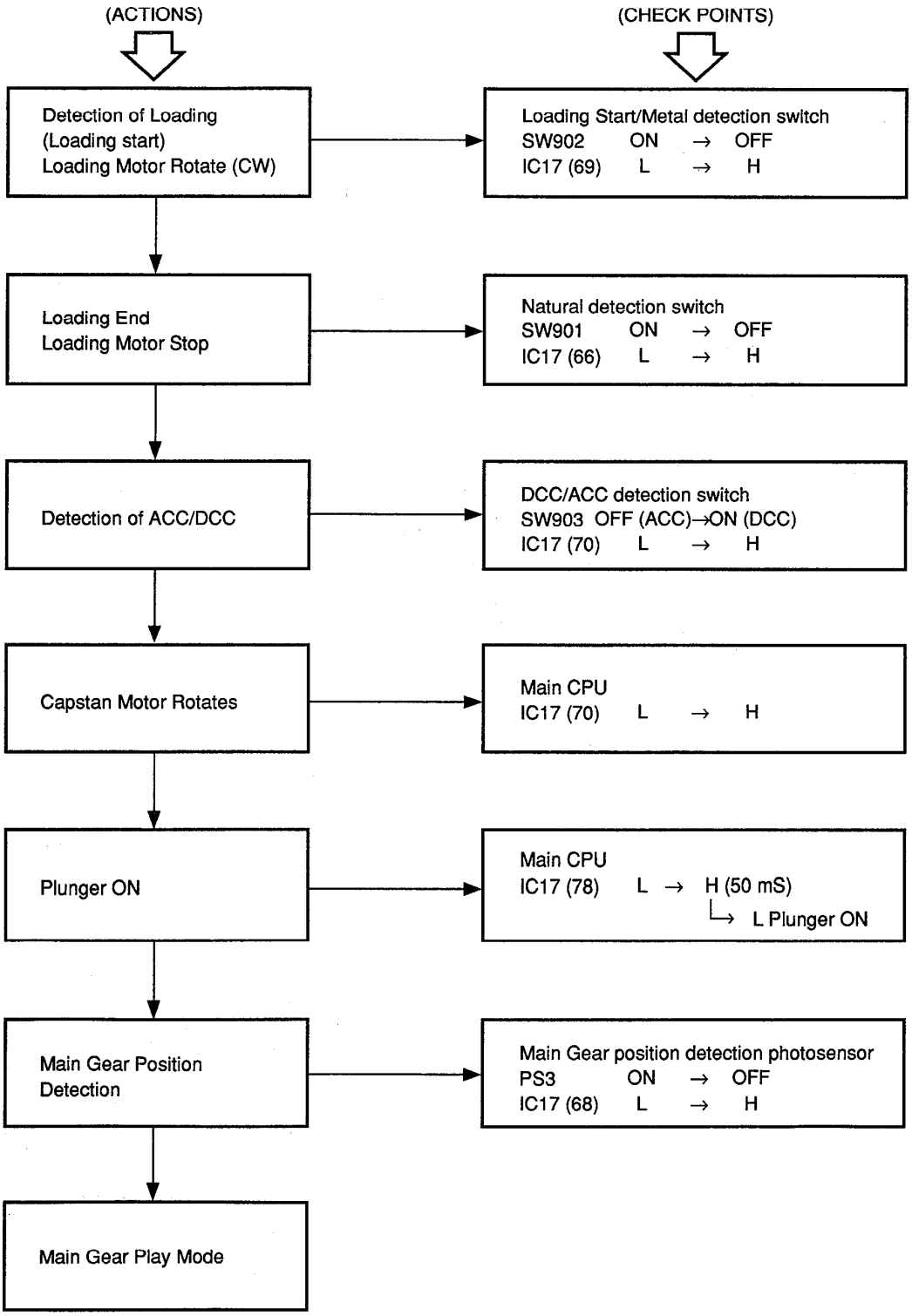
POWER SUPPLY CHART



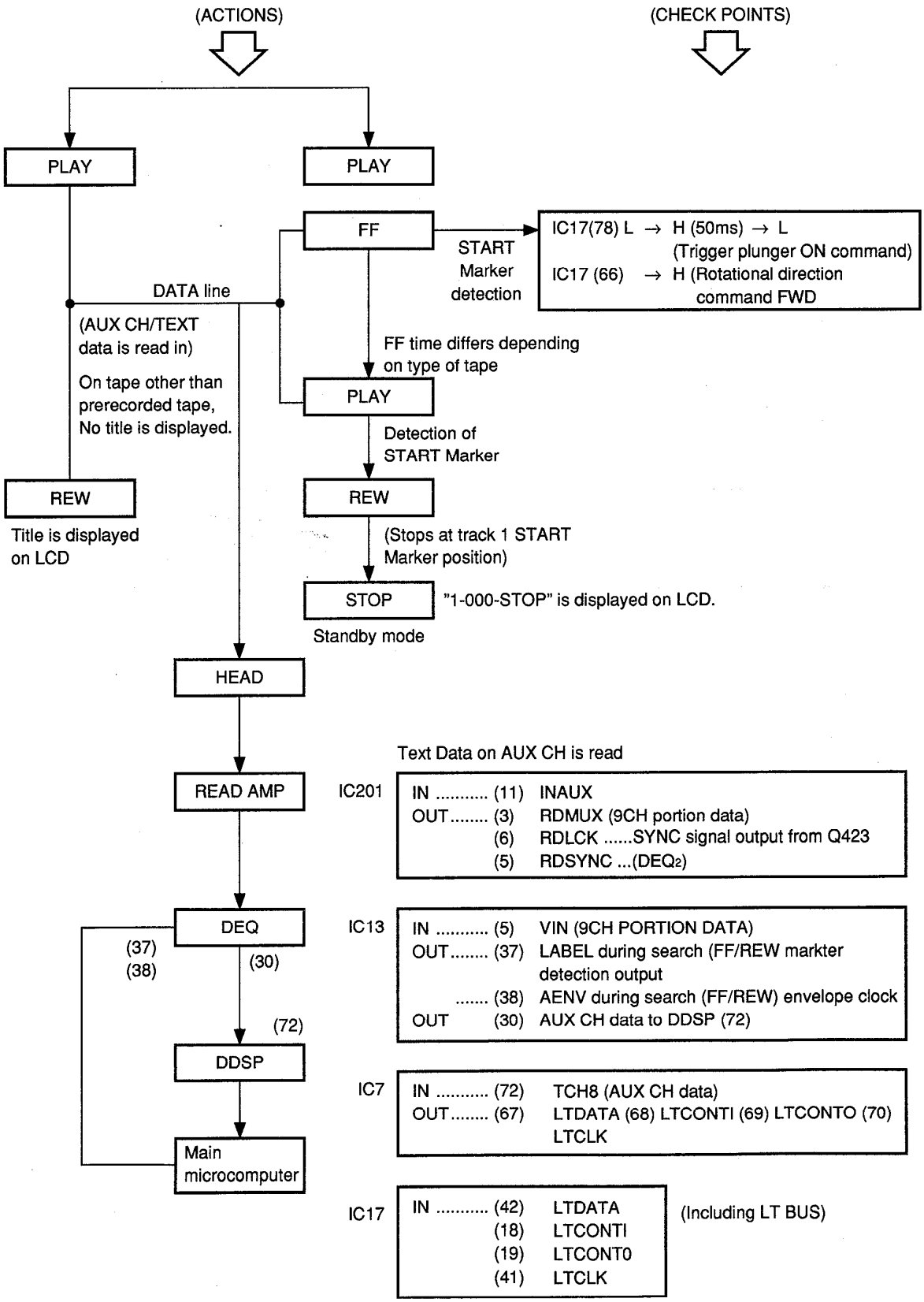
Power Supply Chart



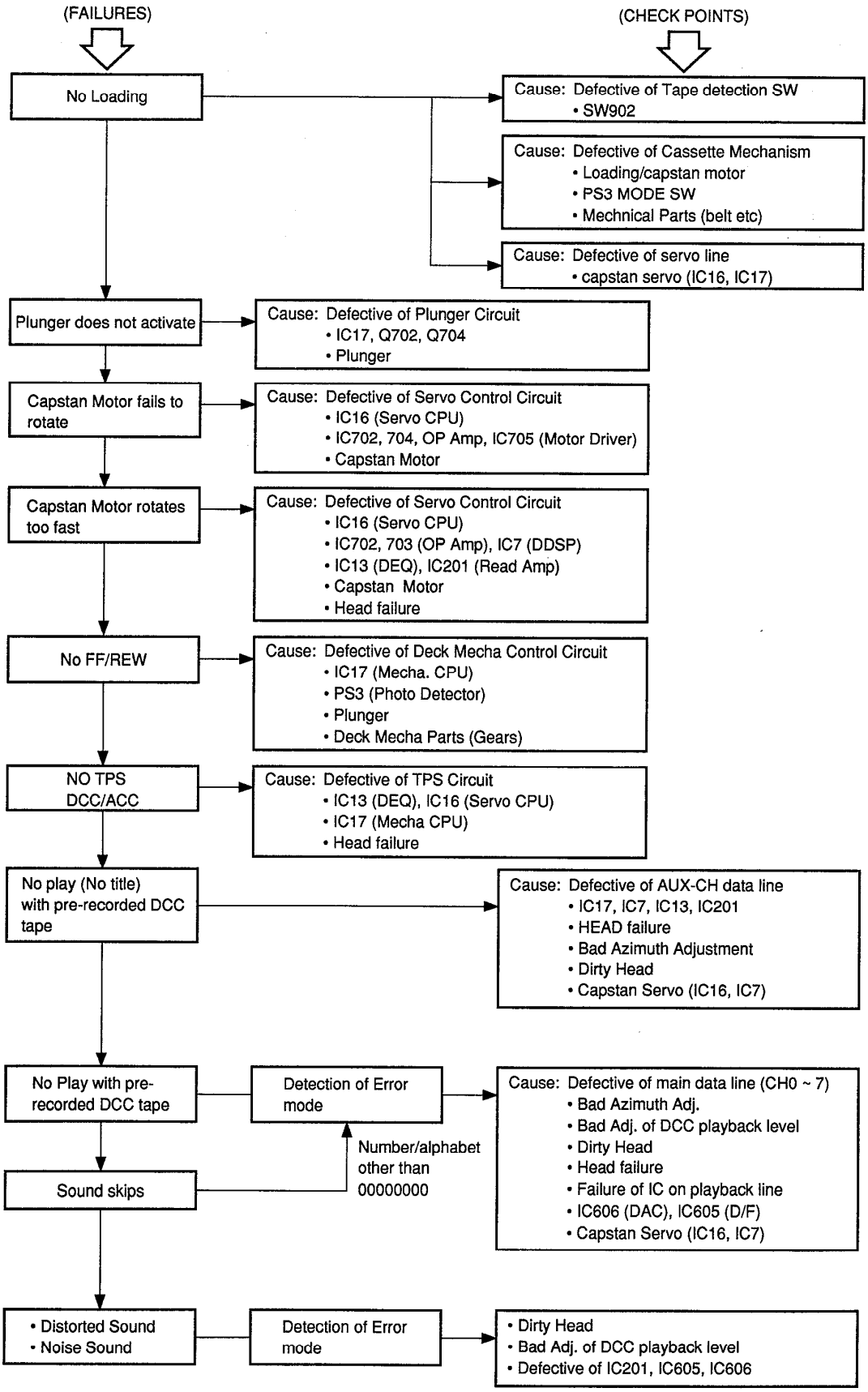
CHECK POINTS IN MECHANISM



CHECK POINTS IN PLAYBACK



CHECK POINTS BY PHENOMENON 1/2


(FAILURES)
(CHECK POINTS)
No Loading
Cause: Defective of Tape detection SW
• SW902
Cause: Defective of Cassette Mechanism
• Loading/capstan motor
• PS3 MODE SW
• Mechnical Parts (belt etc)
Cause: Defective of servo line
• capstan servo (IC16, IC17)
Plunger does not activate
Cause: Defective of Plunger Circuit
• IC17, Q702, Q704
• Plunger
Capstan Motor fails to rotate
Cause: Defective of Servo Control Circuit
• IC16 (Servo CPU)
• IC702, 704, OP Amp, IC705 (Motor Driver)
• Capstan Motor
Capstan Motor rotates too fast
Cause: Defective of Servo Control Circuit
• IC16 (Servo CPU)
• IC702, 703 (OP Amp), IC7 (DDSP)
• IC13 (DEQ), IC201 (Read Amp)
• Capstan Motor
• Head failure
No FF/REW
Cause: Defective of Deck Mecha Control Circuit
• IC17 (Mecha. CPU)
• PS3 (Photo Detector)
• Plunger
• Deck Mecha Parts (Gears)
NO TPS DCC/ACC
Cause: Defective of TPS Circuit
• IC13 (DEQ), IC16 (Servo CPU)
• IC17 (Mecha CPU)
• Head failure
No play (No title) with pre-recorded DCC tape
Cause: Defective of AUX-CH data line
• IC17, IC7, IC13, IC201
• HEAD failure
• Bad Azimuth Adjustment
• Dirty Head
• Capstan Servo (IC16, IC7)
No Play with pre-recorded DCC tape
Detection of Error mode
Cause: Defective of main data line (CH0 ~ 7)
• Bad Azimuth Adj.
• Bad Adj. of DCC playback level
• Dirty Head
• Head failure
• Failure of IC on playback line
• IC606 (DAC), IC605 (D/F)
• Capstan Servo (IC16, IC7)
Number/alphabet other than 00000000
Sound skips
• Distorted Sound
• Noise Sound
Detection of Error mode
• Dirty Head
• Bad Adj. of DCC playback level
• Defective of IC201, IC605, IC606

CHECK POINTS BY PHENOMENON 2/2